

Vegas Schematic

KBL-R

2017/11/08

REV : A00

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DY : None Installed

UMA: UMA only installed

OPS: DISCRTE OPTIMUS installed

<Core Design>



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Title

Cover Page

Size
A4

Document Number

Vegas SKL/KBL-U

Rev

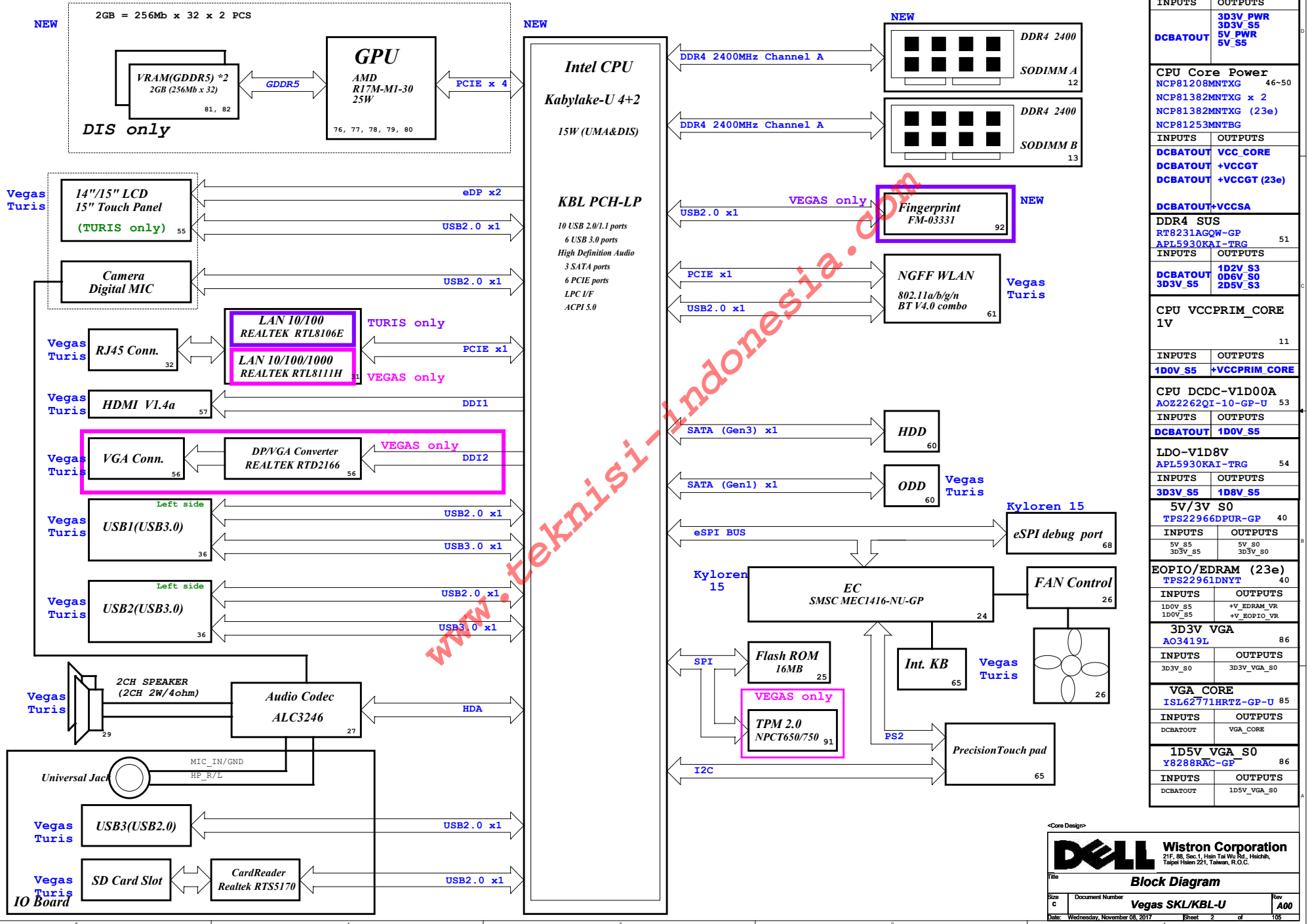
A00

Date: Wednesday, November 08, 2017

Sheet 1 of 105

Project code:
PCB P/N:
Revision: X02

Vegas/Turis MLK KBL-R Block Diagram



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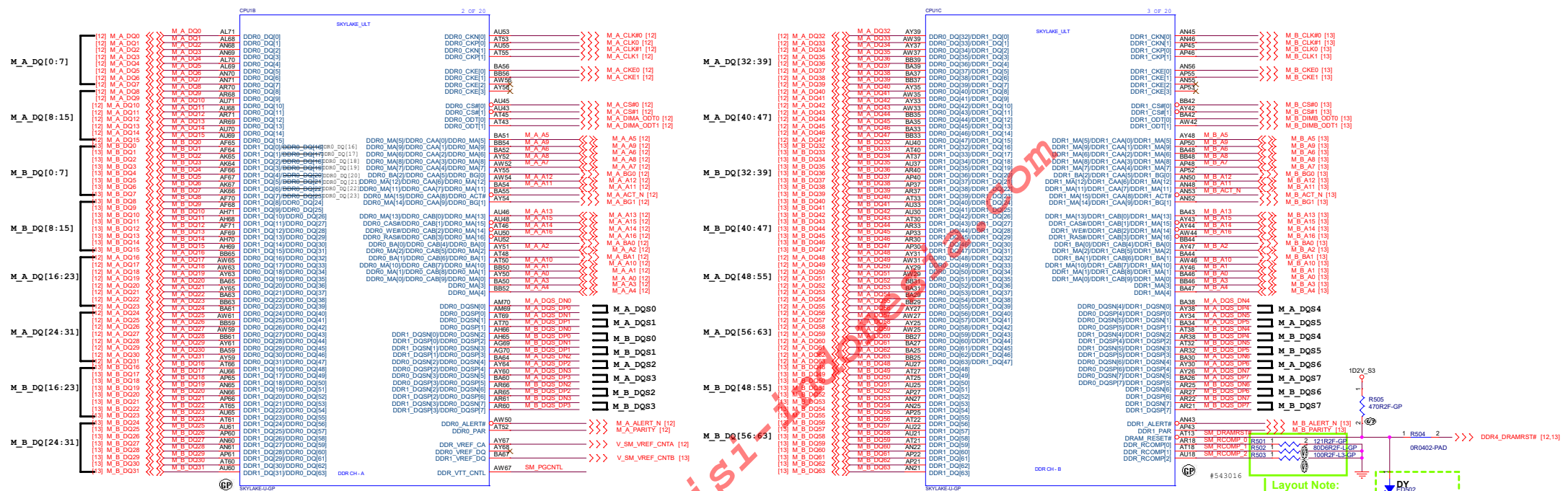
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DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel. Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.

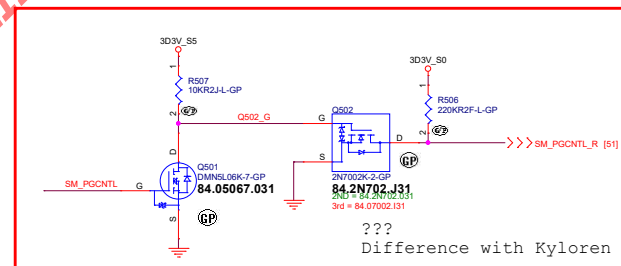
PDG: DDR/ODT

4.17 SKL U and SKL Y System Memory ODT Signal Connectivity Details

Table 4-41. ODT Signal Connectivity table

Processor	Memory	Side	Signal	Rule	Notes
SKL-Y	LPDDR3 Memory Down	Processors	DDR0_ODT[0]	Processor's ODT[0] connected to DRAM's ODT. Topology connection	1,2
			DDR0_ODT[1]	Processor's ODT[1] connected to DRAM's ODT. Topology connection	1,2
SKL-U	LPDDR3 Memory Down	Processors	DDR0_ODT[0]	Processor's ODT[0] connected to DRAM's ODT. Topology connection	1,2
			DDR0_ODT[1]	Processor's ODT[1] connected to DRAM's ODT. Topology connection	1,2
DDR3L Memory Down	Processors	Processors	DDR0_ODT[0]	Processor's ODT[0] connected to DRAM's Rank0 ODT	3,4
			DDR0_ODT[1]	Processor's ODT[1] connected to DRAM's Rank1 ODT	3,4
DDR3L SO-DIMM	Processors	Processors	DDR0_ODT[0]	Processor's ODT[0] connected to DIMM ODT[0]	1,3
			DDR0_ODT[1]	Processor's ODT[1] connected to DIMM ODT[1]	1,3
DDR3L Mixed Memory Down and SO-DIMM	Processors	Processors	DDR0_ODT[0]	Processor's SO-DIMM Channel ODT[0] connected to DIMM ODT[0]	3,4
			DDR0_ODT[1]	Processor's SO-DIMM Channel ODT[1] connected to DIMM ODT[1]	3,4
DDR4 Memory Down	Processors	Processors	DDR0_ODT[0]	Processor's ODT[0] connected to DRAM's Rank0 ODT	3,4
			DDR0_ODT[1]	Processor's ODT[1] connected to DRAM's Rank1 ODT	3,4
DDR4 SO-DIMM	Processors	Processors	DDR0_ODT[0]	Processor's ODT[0] connected to DIMM ODT[0]	1,3
			DDR0_ODT[1]	Processor's ODT[1] connected to DIMM ODT[1]	1,3

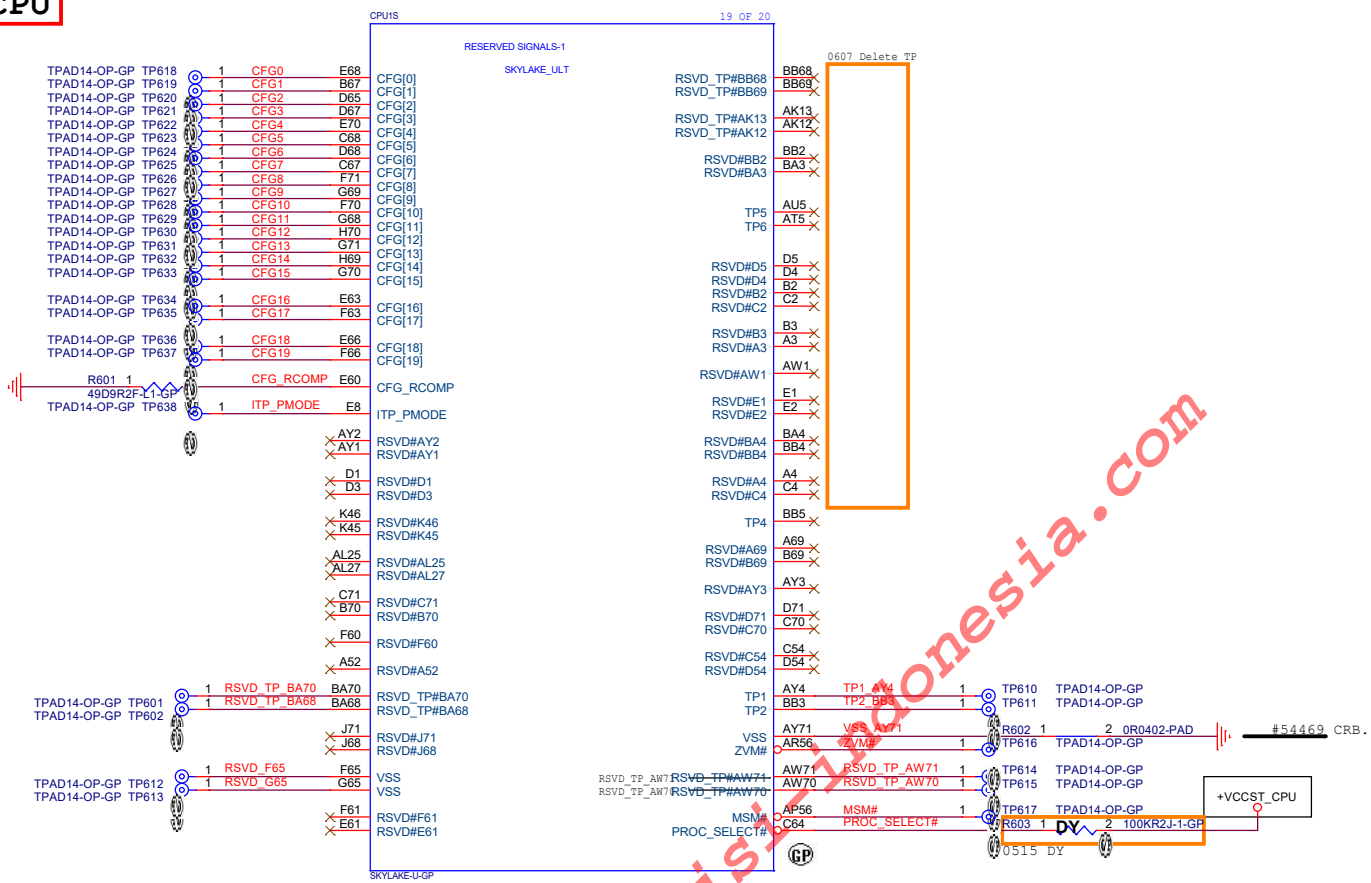
Notes:
1. Additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files (BSP - SKL-Y LPDDR3, BSP - SKL-U LPDDR3).
2. LPDDR3 Rank0 ODT is always enabled by BIOS/UEFI. ODT signal is controlling only Rank0 ODT.
3. DDR3L ODT input is held high (Active). RET_NOM is defined by BIOS as high-2 in both ways, when a Rank receives write command RET_NOM. Left by BIOS after power is stable. Otherwise Left by BIOS after power is stable.
4. These guidelines are related to DDR3L supported Memory down topologies only. 2R x16 DDP single side, 2R x16 SLP dual sided and 2Rx8 dual side.



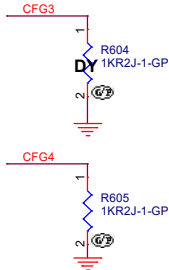
???
Difference with Kyloren

Design Guideline:
SM_RCOMP keep routing length less than 500 mils

Main Func = CPU



PCH strap pin:



[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED
(#543016)	
DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port. 1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

CFG TERMINATIONS

20140807 david

#544669 Rev0.52 (CRB)

SKL(#543016) :
Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

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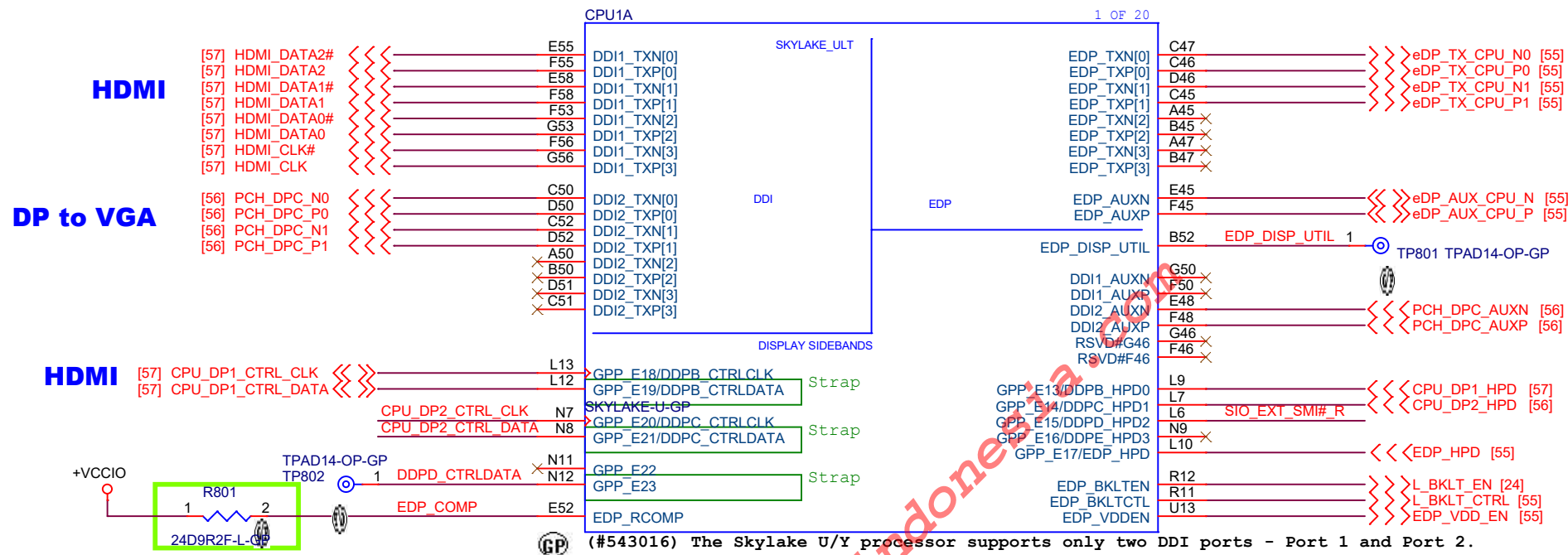
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Title: **CPU (RESERVED)**

Size: A3 Document Number: **Vegas SKL/KBL-U** Rev: **A00**

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Main Func = CPU



(#543016) The Skylake U/Y processor supports only two DDI ports - Port 1 and Port 2.

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 $\pm 1\%$ Ω resistor.

(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω $\pm 1\%$	Max = 100 mils

(#543016) DDI Disabling and Termination Guidelines


Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k $\pm 5\%$ resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k $\pm 5\%$ resistor	NC

Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. * 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. * 1 = Port C is detected.

These two signals have weak internal pull-down.

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Title

CPU (DISPLAY)

Size A4Document Number**Vegas SKL/KBL-U**Rev**A00**

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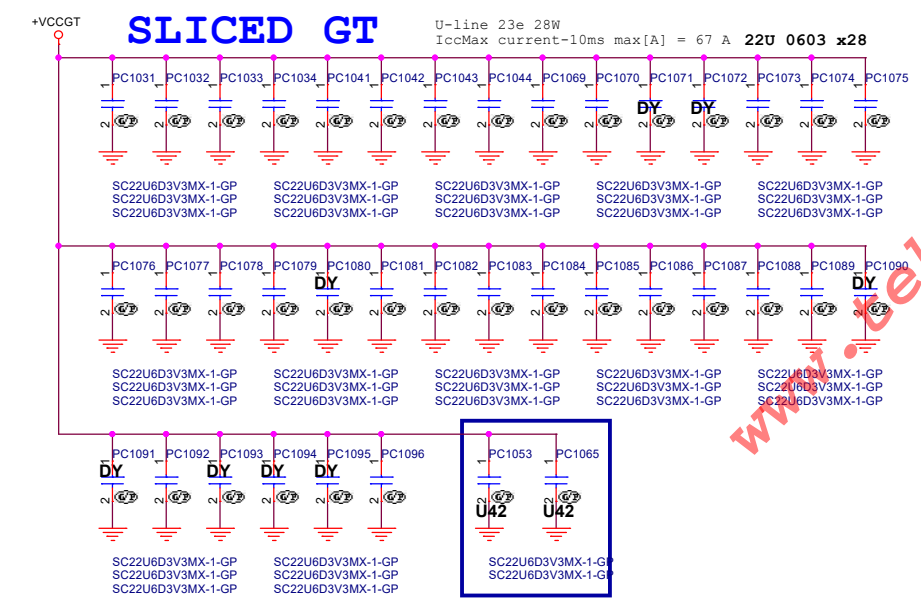
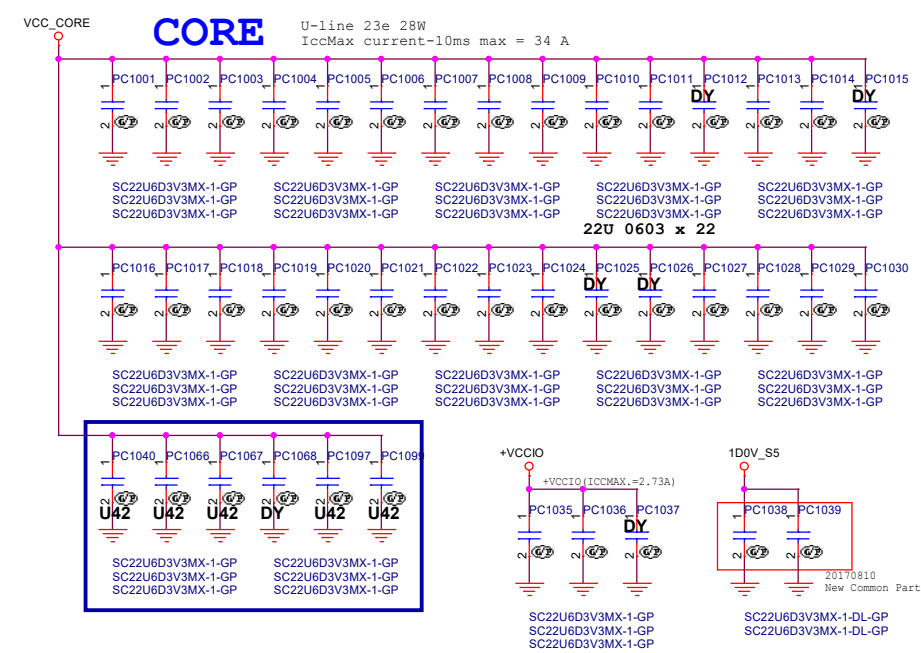
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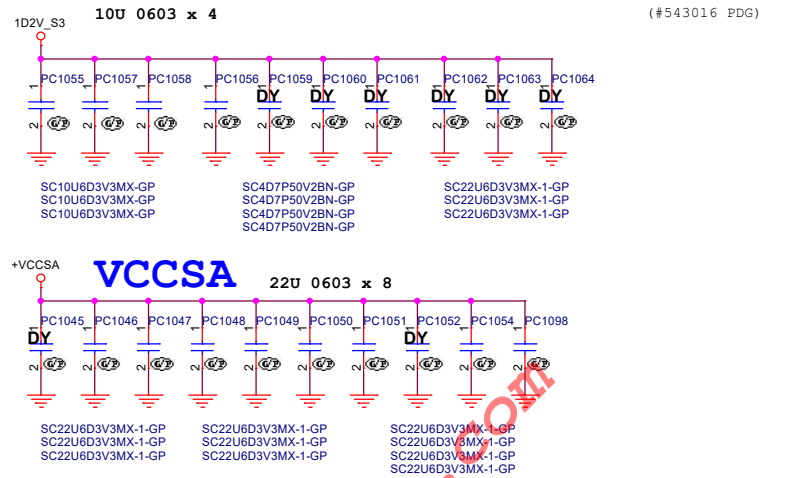
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Title (Reserved)		
Size A4	Document Number Vegas SKL/KBL-U	Rev A00
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Main Func = CPU



KBL-R U42 / KBL U 22 Decoupling Requirements (Sheet 2 of 3)

Domain	Backside cap	Primary side cap	Placement guideline
VCCPLL		1x 1 uF 0402	Place as close to the package as possible.
VCCPLL_DC		1x 1 uF 0201	Do not route VCCPLL, VCCPLL_DC, VCCGT closest adjacent layer over any power net other than ground.
VCCST		1x 1 uF 0402	For VCCST: Refer to Figure 48-2 for additional routing details for VCCST & VCCSTG.



Bulk Decoupling Example (KBL-R U42/KBL U22)

Bulk Decoupling Locations	Example - U 4+2	Example - U 2+2	Notes
Vcc Power Plane at VR output	2x 220 uF (@4.5mΩ ESR)	1x 220 uF (@4.5mΩ ESR)	Placed at primary side near to VR output
VccGT Power Plane at VR output	2x 220 uF (@4.5mΩ ESR)		Placed at backside side near to VR output
VDDQ Power Plane at VR output		2x 47 uF 0805	Placed at primary side near to VR output
VCCIO Power Plane at VR output		2x 47 uF 0805	Placed at primary side near to VR output
VCCSA Power Plane at VR output		2x 47 uF 0805	Placed at primary side near to VR output
VCCPLL Power Plane at V1P0A VR output		1x 0.1uF 0402	Placed at primary side near to VR output

Notes:
1. These examples are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.
2. Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

KBL-R U42 / KBL U 22 Decoupling Requirements (Sheet 1 of 3)

Domain	Backside cap	Primary side cap	Placement guideline
Vcc	7x 10 uF 0402		Place on secondary side, underneath the package
	31x 1 uF 0402 or 0201		Refer to diagram in Note 4 below for placement recommendation of 0402 caps Refer to diagram in Note 5 below for placement recommendation of 0201 caps
		9x 22 uF 0603	Place as close to the package as possible
		8x 47 uF 0805 (6.3V) ¹	
		8x 10 uF 0402	
Vcc/VccGT	5x 1 uF 0402 or 0201		Place as close to the package as possible
VCCGT	12x 10 uF 0402		Place on secondary side, underneath the package
		7x 22 uF 0603	Place as close to the package as possible
		3x 47 uF 0805 (6.3V) ¹	
VCCSA	7x 10 uF 0402		Place on secondary side, underneath the package
	7x 1 uF 0402 or 0201		
VCCIO	6x 10 uF 0402		Place as close to the package as possible
	4x 1 uF 0402		Place as close to the package as possible
VDDQ	4x 10 uF 0402		Place as close to the package as possible
	3 x 22 uF 0603		Place as close to the package as possible
VDDQC		1 x 10 uF 0402	Preferred to place the 0402 10uF cap on the secondary under the package shadow near VDDQC pin and short to VDDQ rail under with a shape. Alternatively, if the 0402 cap cannot be placed on the backside, follow the example showed in Figure 48-3. The 0402 cap to VDDQC BGA routing should not exceed 48mm (RdC). RVP design uses trace L=450mil, W=8mil between BGA and cap. Additional trace routing implemented in RVP design was not required.

Note: Refer to latest revision of KBL- RU PDG for final specifications

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Title: **CPU (Power CAP1)**

Size A3 Document Number **Vegas SKL/KBL-U** Rev **A00**

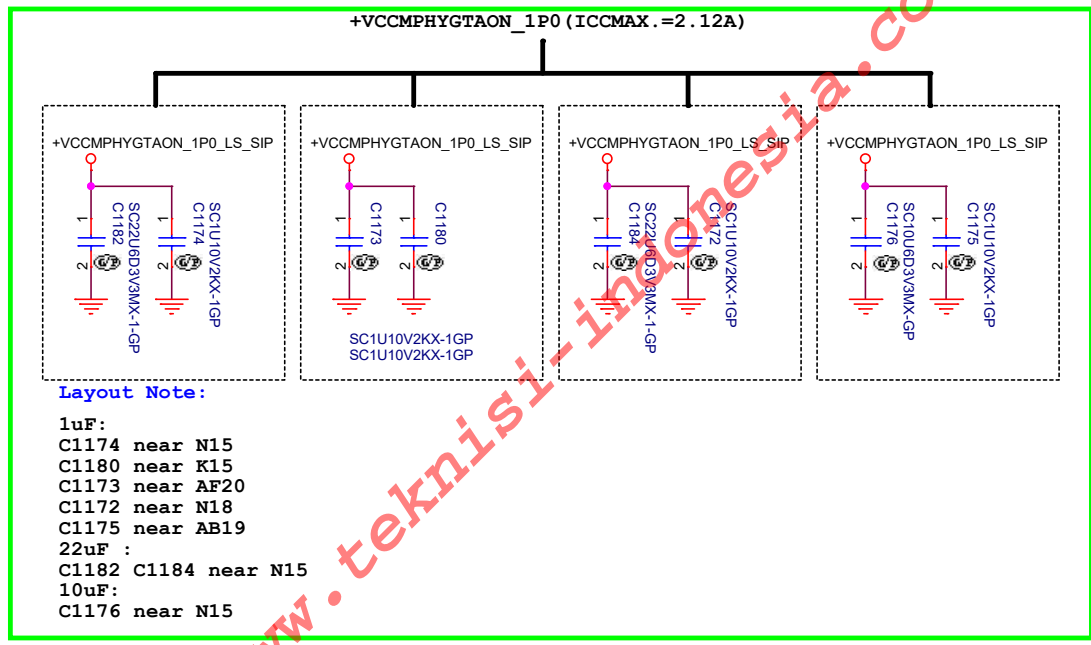
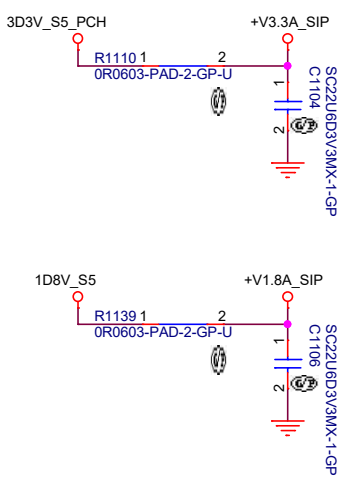
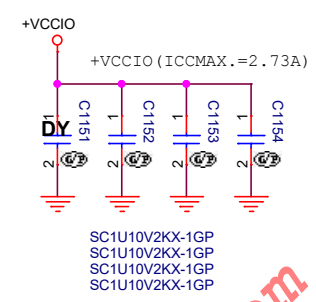
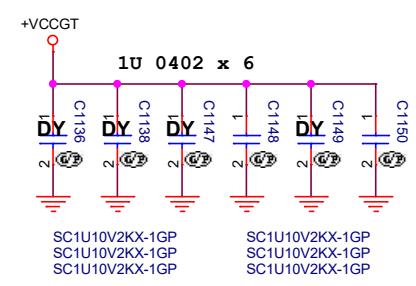
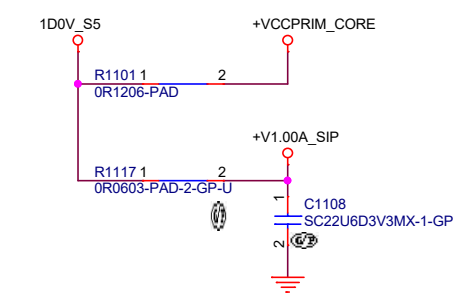
Date: Wednesday, November 08, 2017 Sheet 10 of 105

Main Func = CPU

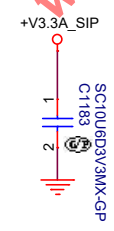
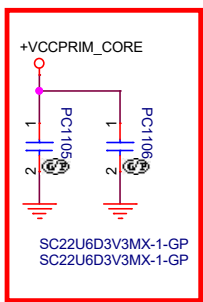
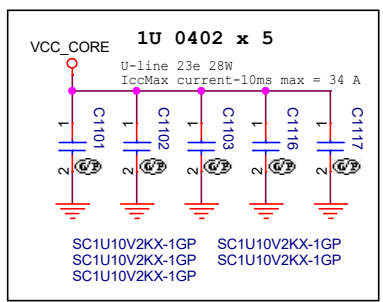
PCH DERIVED RAILS

UNSLICED GT

VCCIO



Layout Note:
1uF:
C1174 near N15
C1180 near K15
C1173 near AF20
C1172 near N18
C1175 near AB19
22uF :
C1182 C1184 near N15
10uF:
C1176 near N15

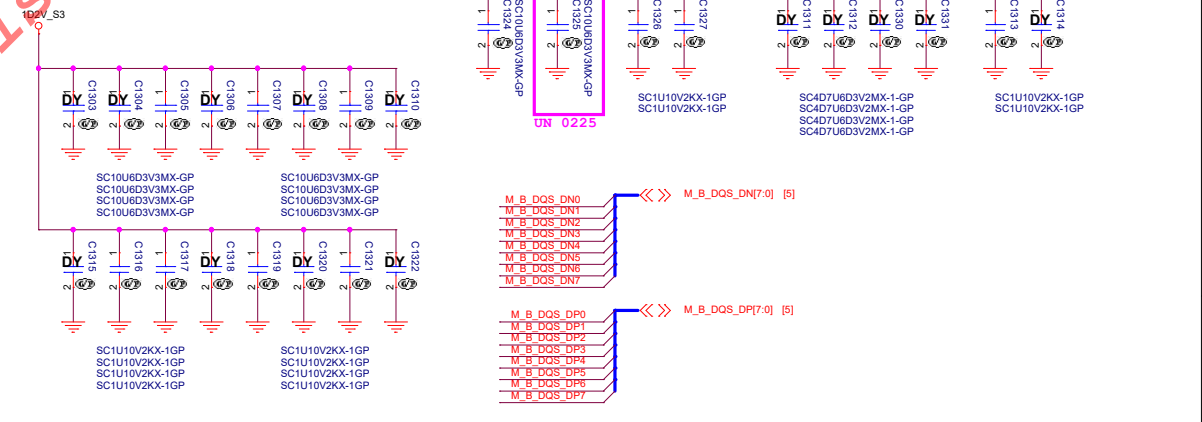
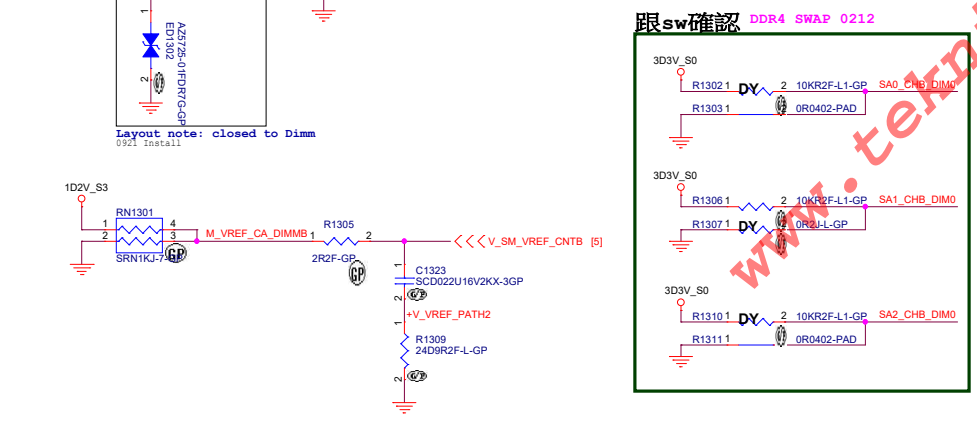
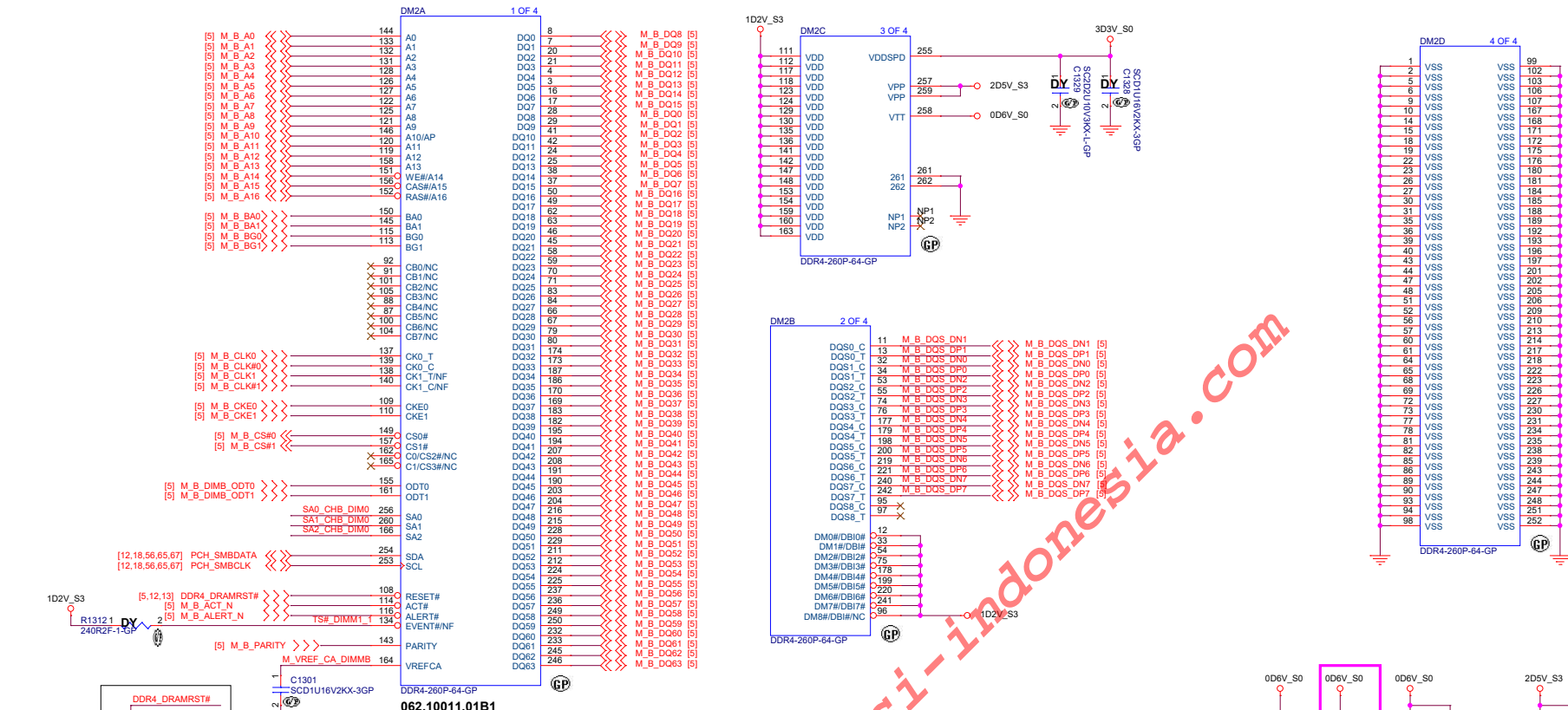


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Title CPU (Power CAP2)			
Size Custom	Document Number Vegas SKL/KBL-U		Rev A00
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Main Func = DDR4 SODIMM

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062.10011.01B1



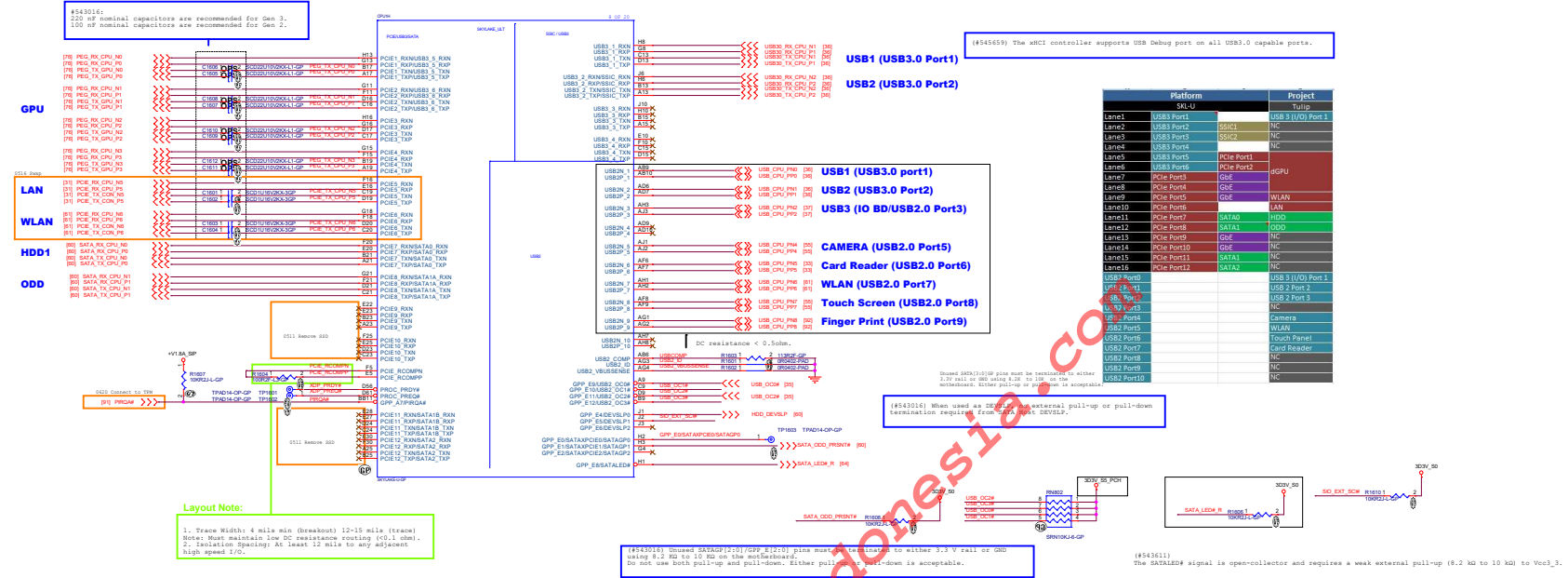
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Title (Reserved)_SODIMM _SODIMM4		
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(#545659) The xHCI controller supports USB Debug port on all USB3.0 capable ports.
```



	Platform	Project
	SKU-U	Tulip
Lane0	USB8 Port1	USB 3 (I/O) Port 1
Lane2	USB8 Port3	NC
Lane3	USB8 Port4	NC
Lane4	USB8 Port6	NC
Lane5	USB8 Port7	NC
Lane6	USB8 Port8	PCIe Port2
Lane7	PCIe Port3	GPU
Lane8	PCIe Port4	GPU
Lane9	PCIe Port5	GPU
Lane10	PCIe Port6	WI-FI
Lane11	PCIe Port7	SSD
Lane12	PCIe Port8	SSD
Lane13	PCIe Port9	GPU
Lane14	PCIe Port10	GPU
Lane15	PCIe Port11	NC
Lane16	PCIe Port12	NC
USB Port1		USB 3 (I/O) Port 1
USB Port2		USB 3 (I/O) Port 2
USB Port3		NC
USB Port4		NC
USB Port5		Camera
USB Port6		WI-FI
USB Port7		Touch Panel
USB Port8		Cad Reader
USB Port9		NC
USB Port10		NC

PCIe Table

Port	Device	Share BUS
1	N/A	USB3_0_3
2	N/A	USB3_0_4
3	WLAN	
4	LAN	
5 (LO-L3)	GPU	
6 (L3)	HDD	SATA0
6 (L2)	ODD	SATA1
6 (LO-L1)	N/A	

USB 2.0 Table

Pair	Device
0	USB3.0 port1
1	USB3.0 Port2
2	USB2.0 Port3 (IOMD)
3	Finger Print
4	CAMERA
5	Card Reader
6	Touch Panel
7	WLAN

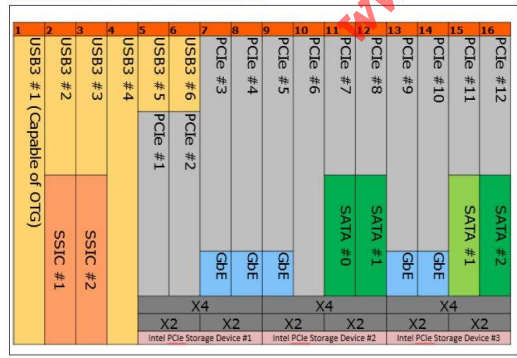
Table 24-2. PCI Express* Port Feature Details

SKL	Max Device (Ports)	Max Lanes	PCIe+ Gen Type	Encoding	Transfer Rate (MT/s)	Theoretical Max Bandwidth (GB/s)			
						x1	x2	x4	
U	6	12	1	8b/10b	2500	0.25	0.50	1.00	
			2	8b/10b	5000	0.50	1.00	2.00	
			3	128b/130b	8000	1.00	2.00	3.94	
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00	
			2	8b/10b	5000	0.50	1.00	2.00	

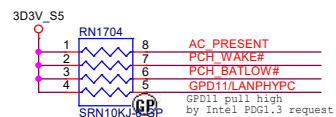
Table 24-3. PCI Express* Link Configurations Supported

SKL	PCIe Link Config	PCI Express* Lanes											
		1	2	3	4	5	6	7	8	9	10	11	12
U	1x4	Port1				Port5				Port9			
	2x2	Port1		Port3		Port5		Port7		Port9		Port11	
	1x2 + 2x1	Port1		Port3		Port5		Port7		Port9		Port11	
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11	Port12
Y	1x4	Port1				Port5							
	2x2	Port1		Port3		Port5		Port7					
	1x2 + 2x1	Port1		Port3		Port5		Port7					
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8				
	1x2									Port9			
	2x1									Port9	Port10		

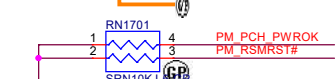
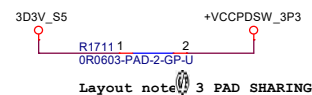
Figure 3-1. HSIO Muxing on SKL PCH-LP (U Series)



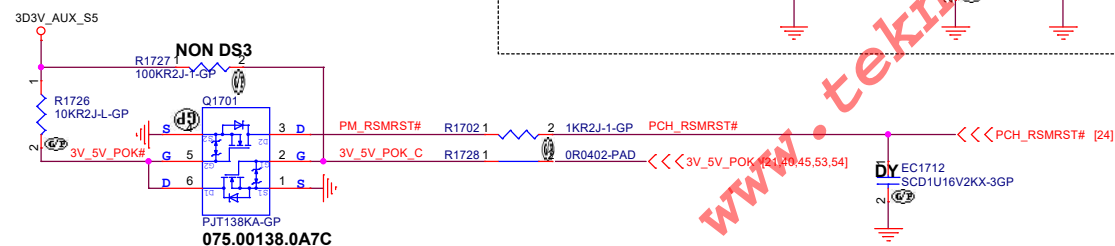
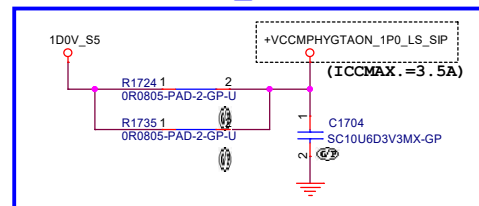
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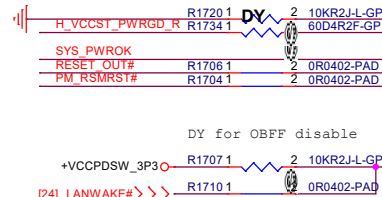
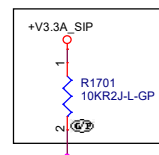
BATLOW#:
Pull-up required even if not implemented.



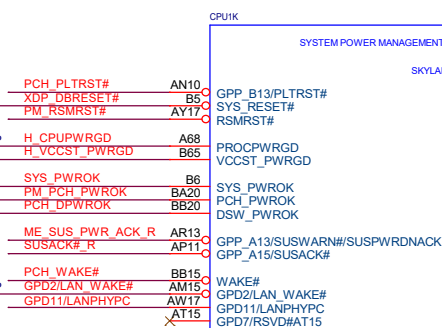
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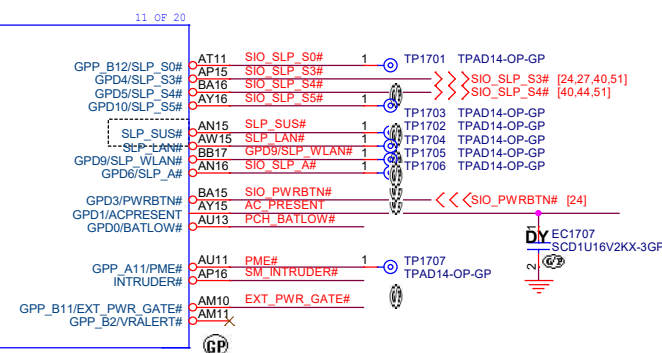
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[24] SYS_PWROK    >>> _____
[24,26,79] RESET_OUT# >>>> _____
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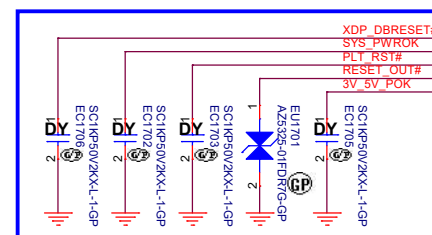
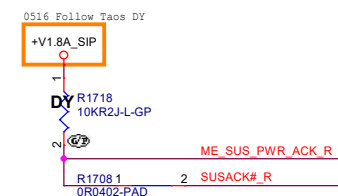
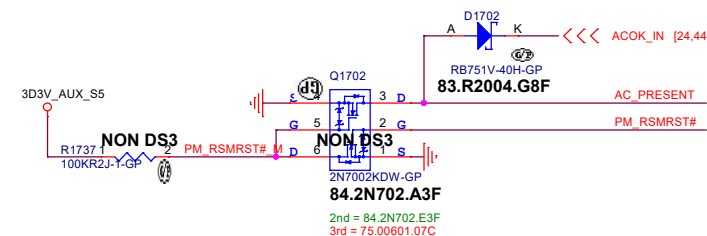
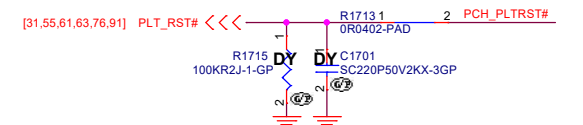
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WAKE#: Ensure that WAKE# signal Trise (Maximum) is <100 ns.



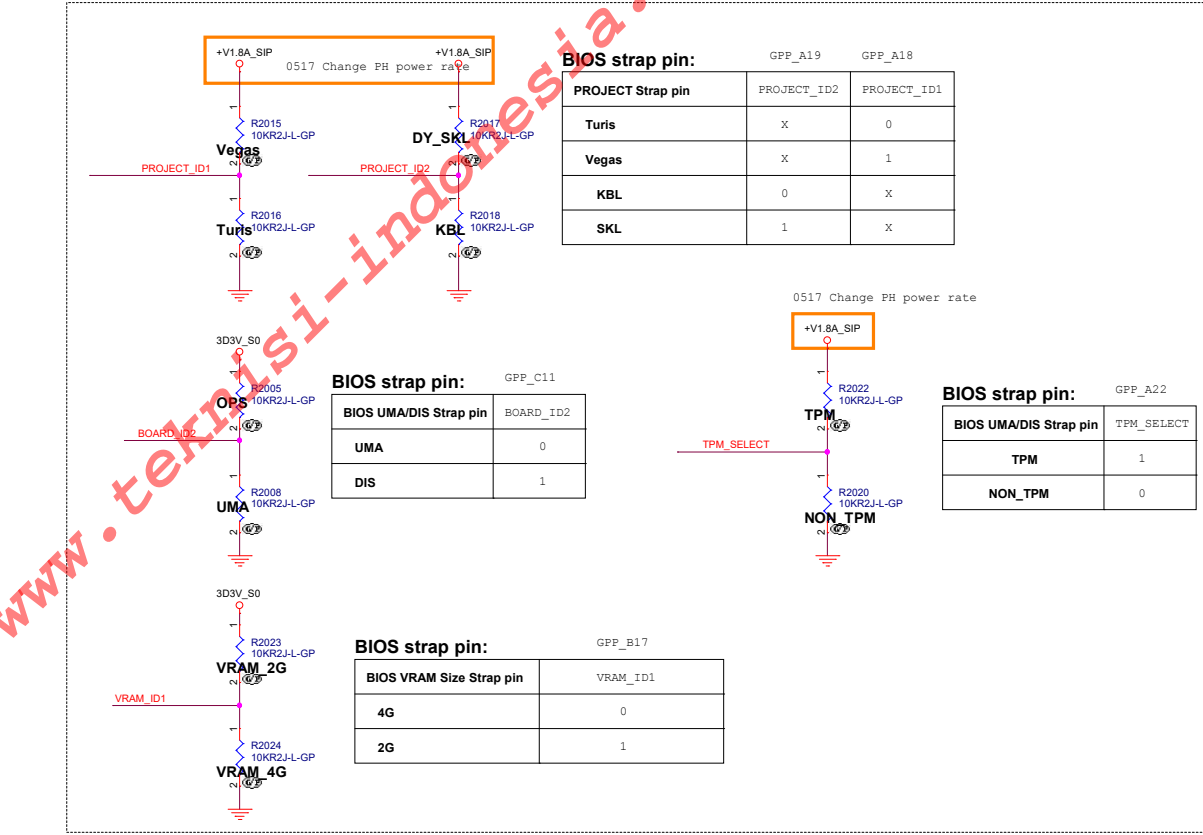
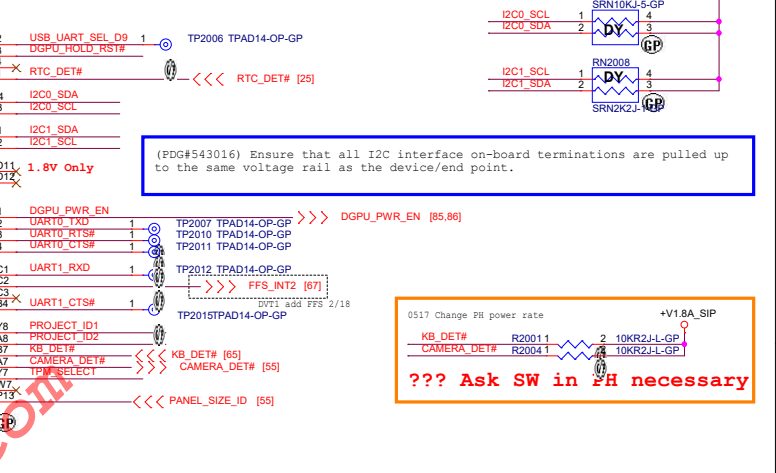
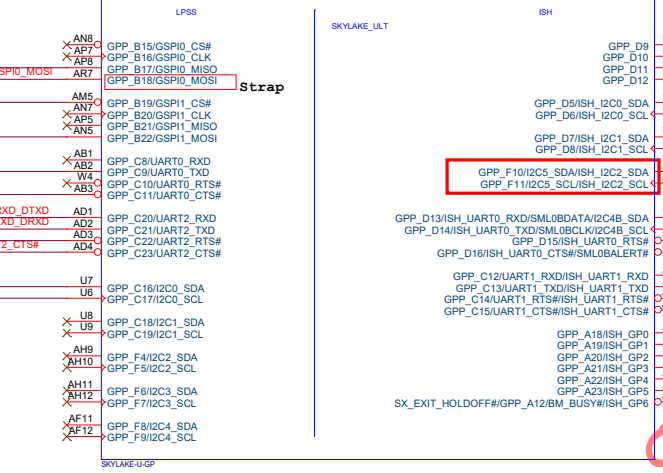
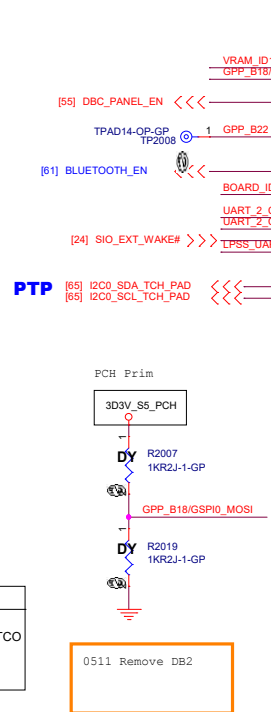
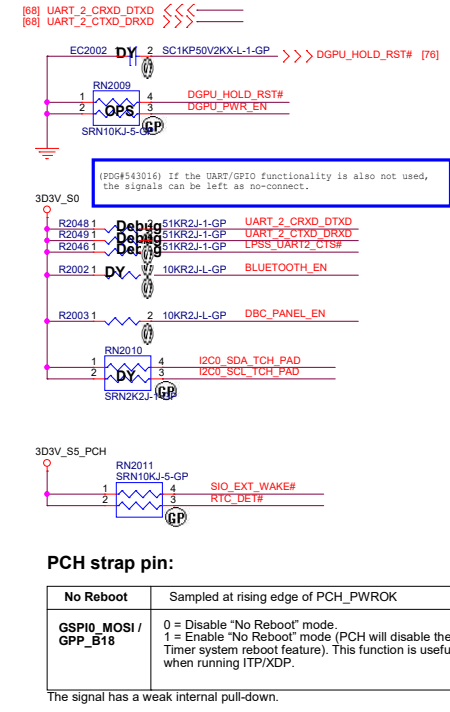
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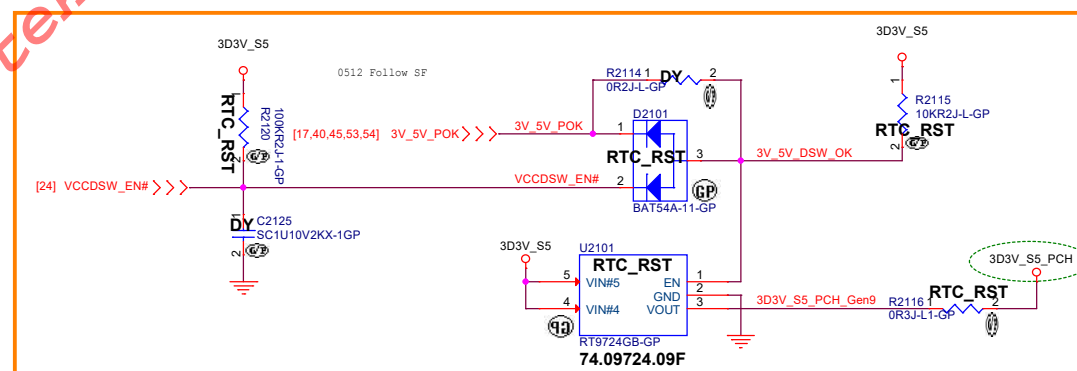
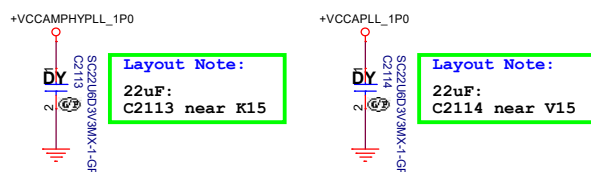
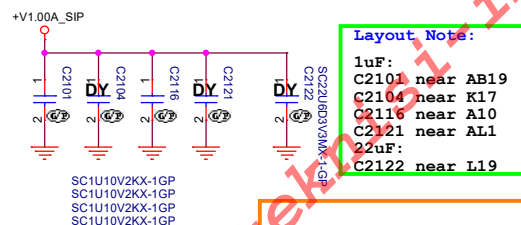
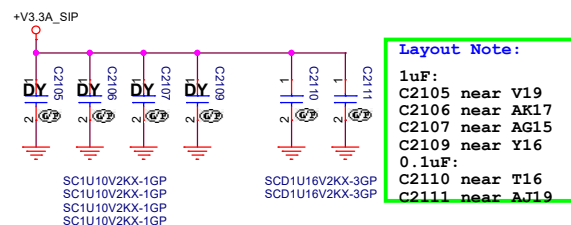
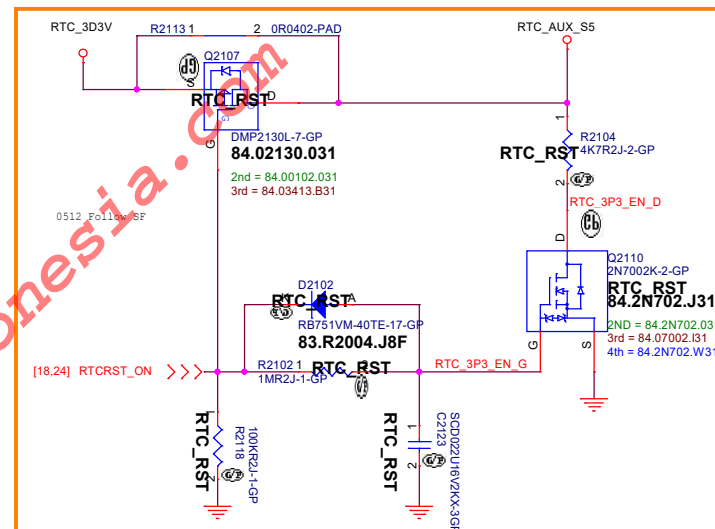
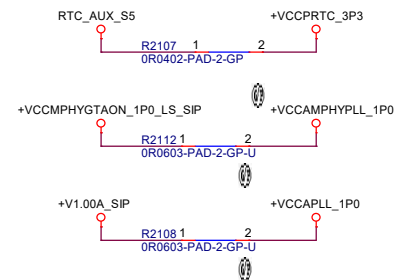
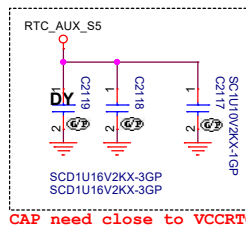
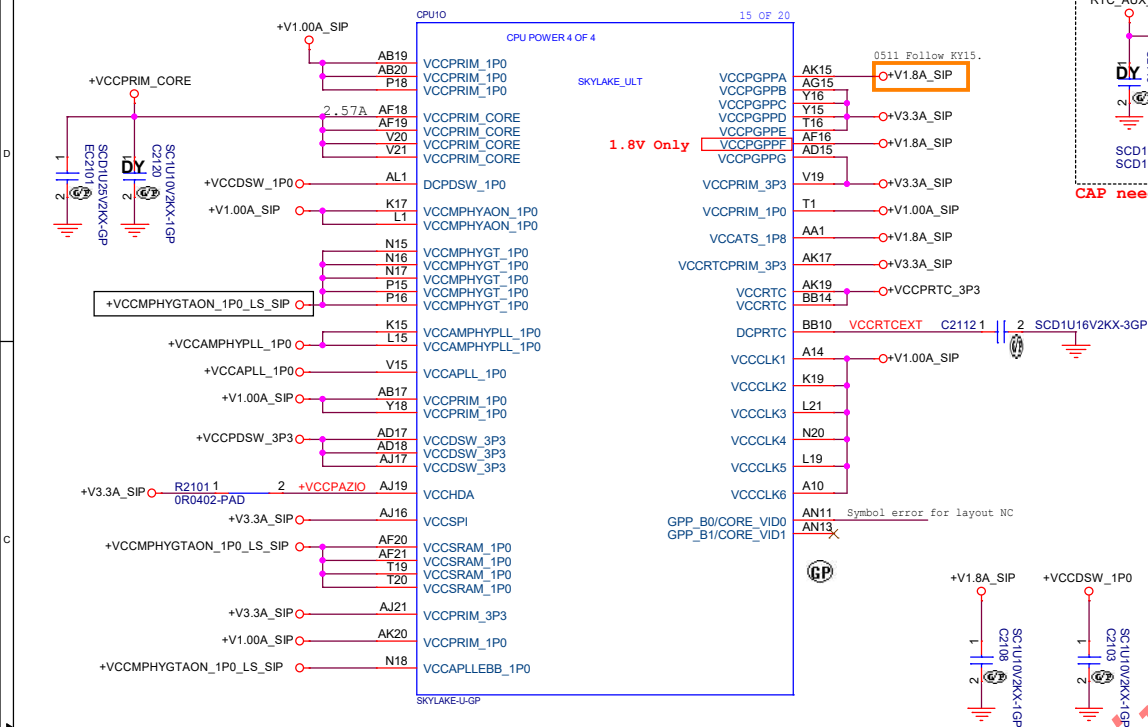
```
[#543016 Rev0.7]
EXT_PWR_GATE# : Due to a bug on A0, a temporary pull-up resistor will be required to overcome the internal 20k
pull-down that is active during the early portion of the power up sequence
```



Main Func = PCH

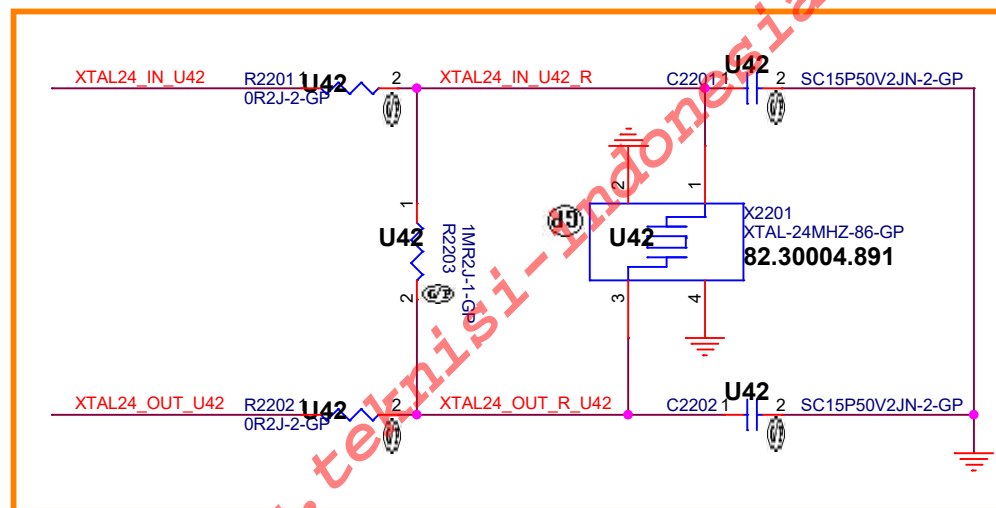
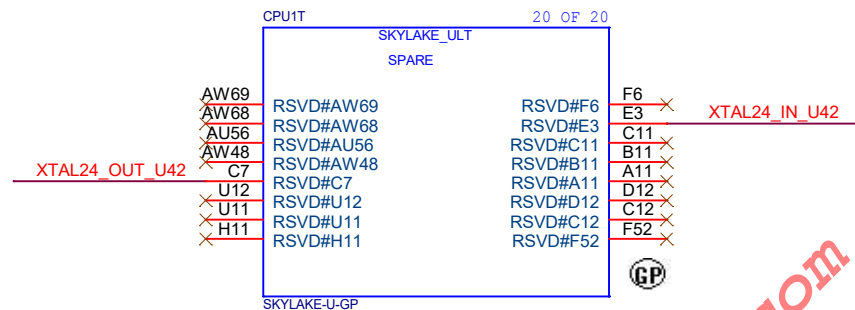


Main Func = PCH



Main Func = PCH

20170427



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Title

CPU_(RSVD)

Size
A4

Document Number

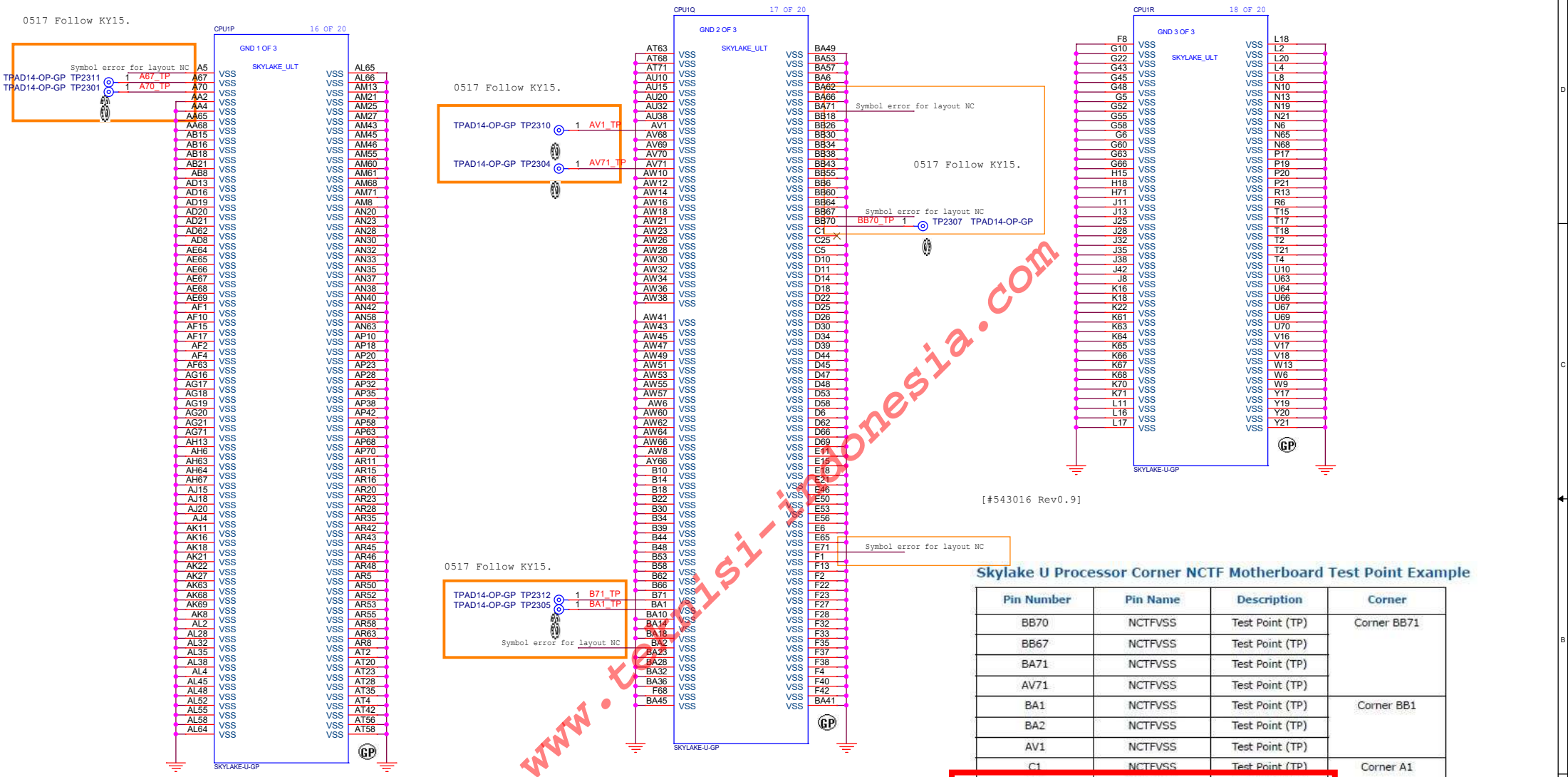
Vegas SKL/KBL-U

Rev
A00

Date: Wednesday, November 08, 2017

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Main Func = PCH



Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	Corner BB1
BA1	NCTFVSS	Test Point (TP)	
BA2	NCTFVSS	Test Point (TP)	Corner A1
AV1	NCTFVSS	Test Point (TP)	
C1	NCTFVSS	Test Point (TP)	Corner A71
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

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Title

CPU (VSS)

Size A3

Document Number

Vegas SKL/KBL-U

Rev **A00**

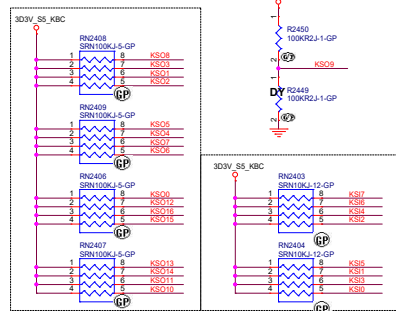
Date: Wednesday, November 08, 2017

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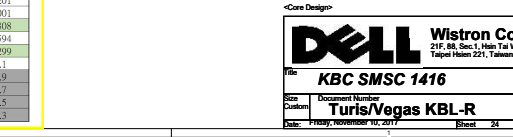
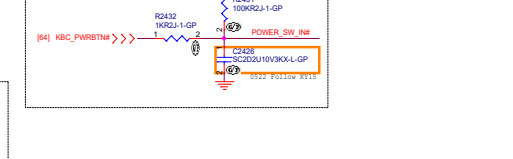
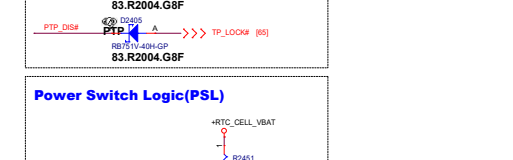
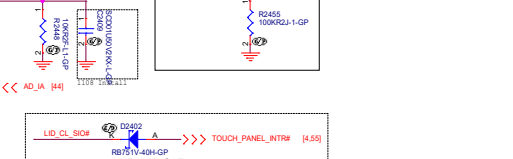
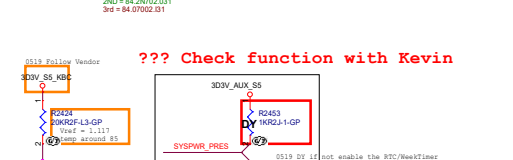
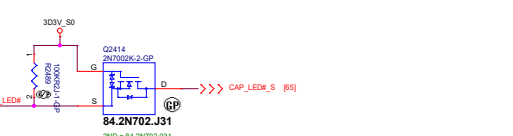
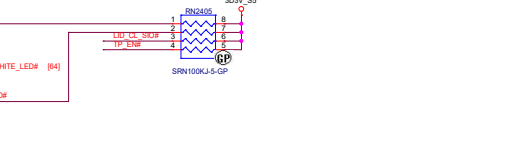
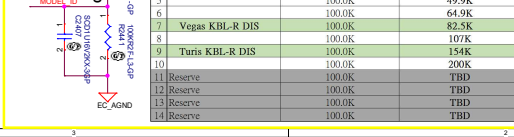
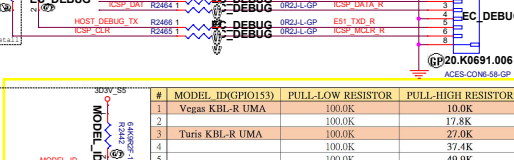
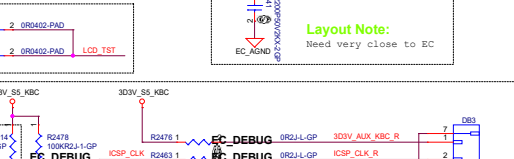
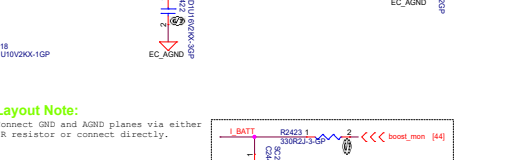
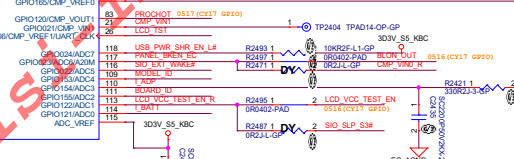
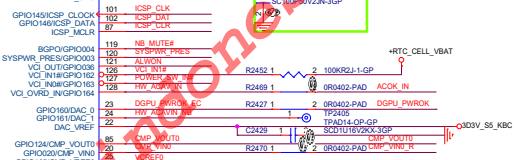
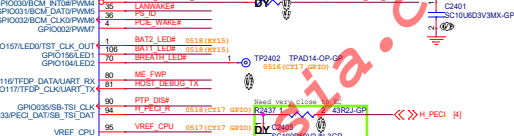
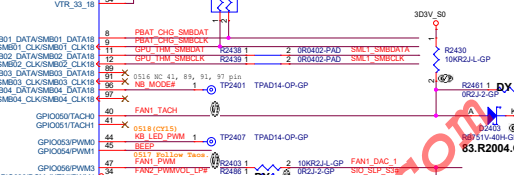
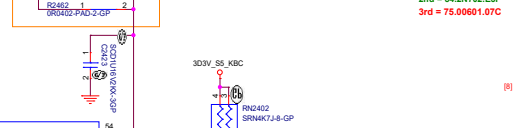
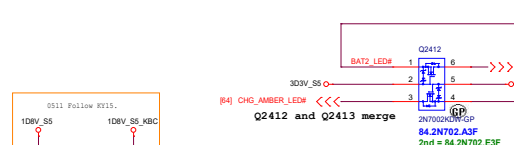
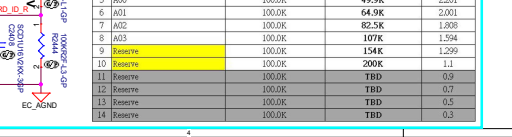
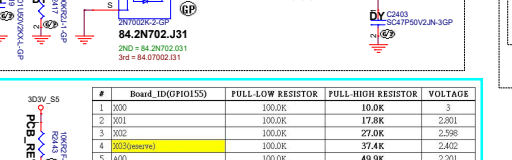
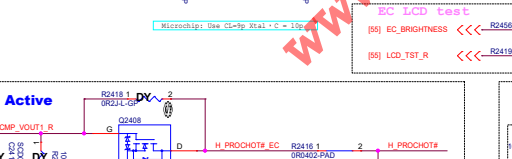
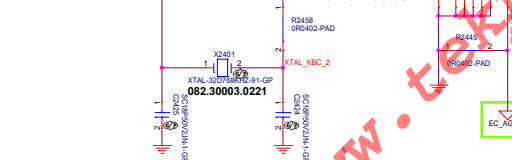
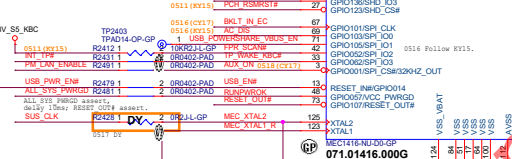
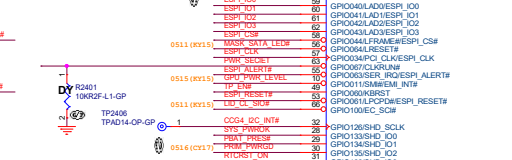
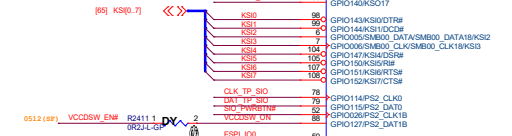
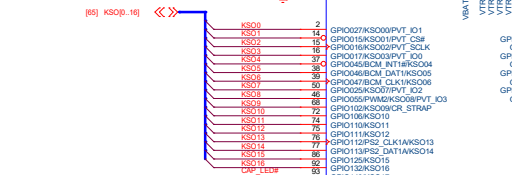
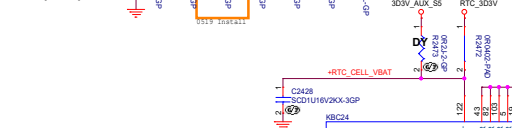
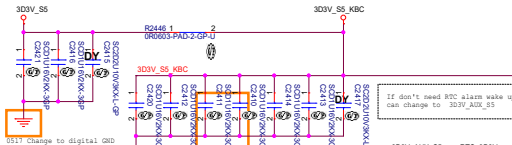
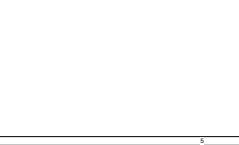
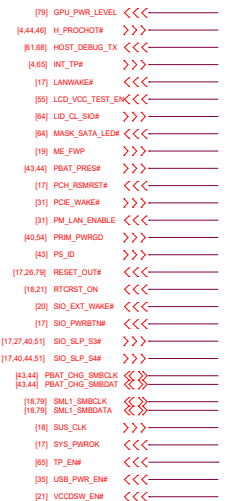
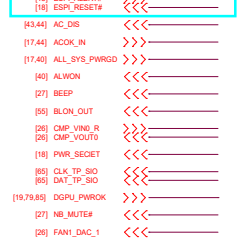
Main Func = KBC

Layout Note:

Need very close to EC



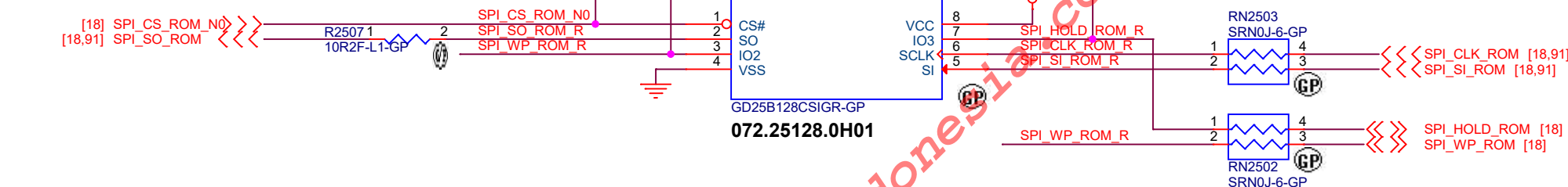
ESPI



#	board_ID(GPIO55)	PULL-UP RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	0000	1000K	10.0K	3
2	0011	1000K	17.8K	2.801
3	0012	1000K	27.0K	2.598
4	0013 (overrun)	1000K	27.4K	2.632
5	0000	1000K	69.9K	2.001
6	0011	1000K	64.9K	2.201
7	0012	1000K	82.5K	1.809
8	0013	1000K	107K	1.594
9	0000	1000K	150K	1.299
10	Reserve	1000K	200K	1.1
11	Reserve	1000K	TBD	0.9
12	Reserve	1000K	TBD	0.7
13	Reserve	1000K	TBD	0.5
14	Reserve	1000K	TBD	0.3

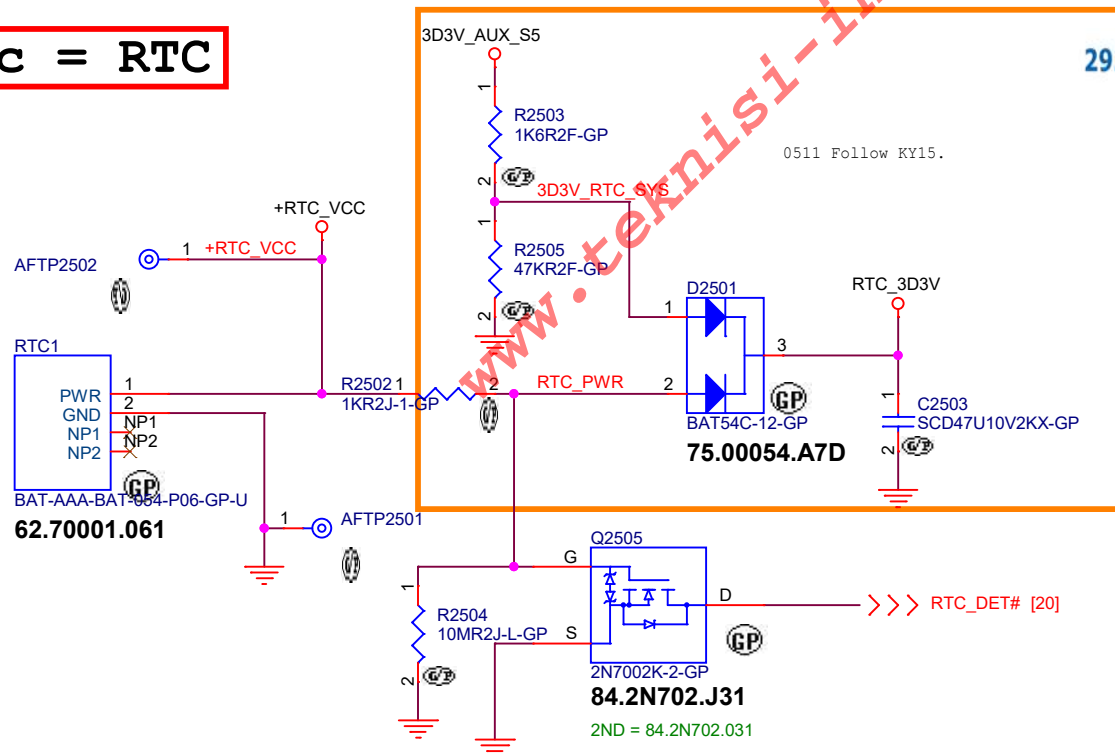
#	MODEL	INDG(P133)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	Vegas KBL-R UMA	100.0K	10.0K	3	
2		100.0K	17.8K	2.801	
3	Turis KBL-R UMA	100.0K	27.0K	2.598	
4		100.0K	37.4K	2.402	
5		100.0K	49.9K	2.201	
6		100.0K	64.9K	2.002	
7	Vegas KBL-R DIS	100.0K	82.5K	1.808	
8		100.0K	107K	1.594	
9	Turis KBL-R DIS	100.0K	154K	1.299	
10		100.0K	200K	1.1	
11	Reserve	100.0K	TBD	0.9	
12	Reserve	100.0K	TBD	0.7	
13	Reserve	100.0K	TBD	0.5	
14	Reserve	100.0K	TBD	0.3	

Main Func = RTC



29.2.1 VCCRTC External Circuit

On KBL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V. The following sections will detail various options platform designers can use to achieve this new specification.



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Title

Flash/RTC

Size

Document Number

Turis/Vegas KBL-R

Rev

A00


Date: Wednesday, November 08, 2017

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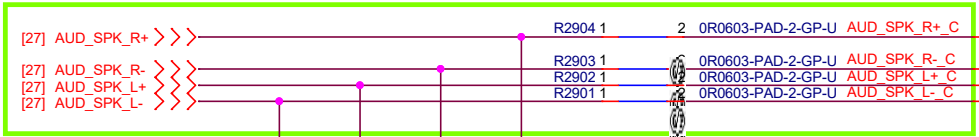
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Size A4	Document Number Vegas SKL/KBL-U		Rev A00
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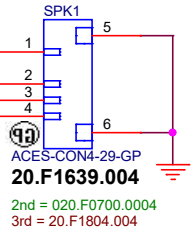
Main Func = Audio

Layout Note:

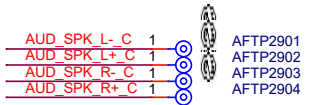
Speaker trace width >40mil @ 2W4ohm speaker power



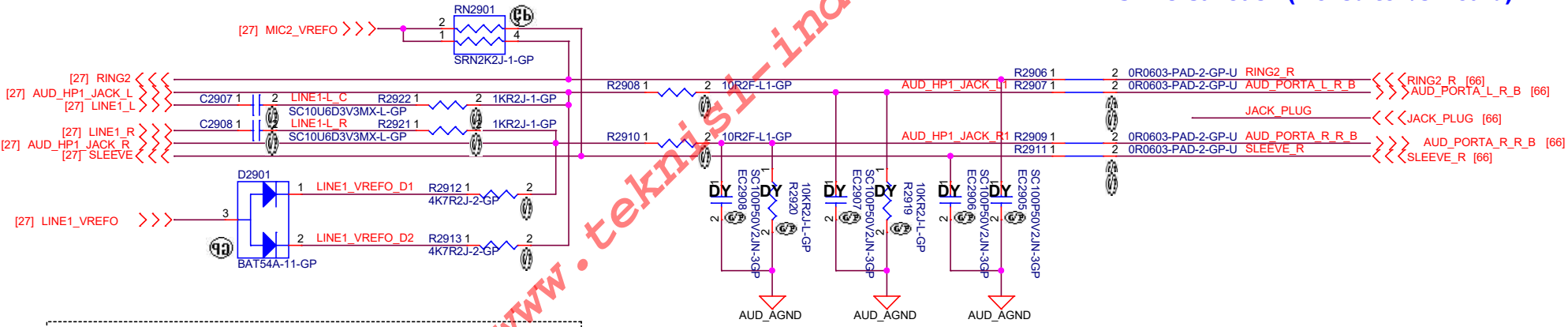
Speaker



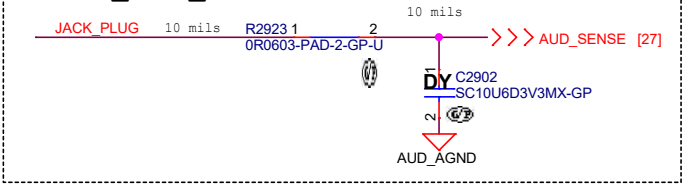
CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-



Universal Jack (Moved to I/O Board)



Delay circuit
(JACK_PLUG_DET: on IO Board)



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Title

Audio IO

Size Custom

Document Number

Turis/Vegas KBL-R

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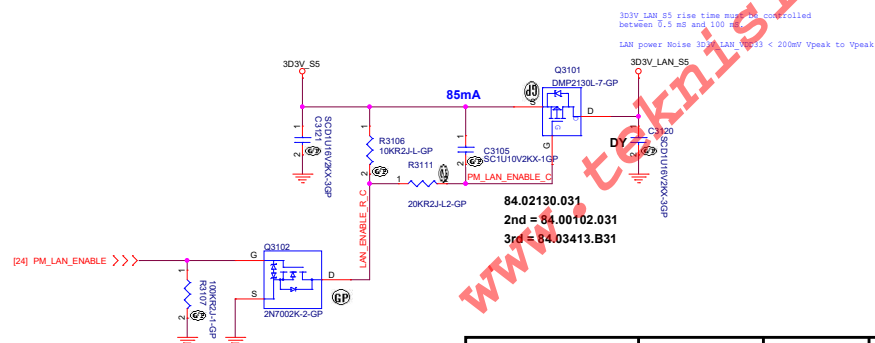
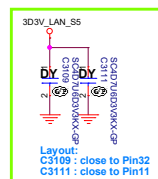
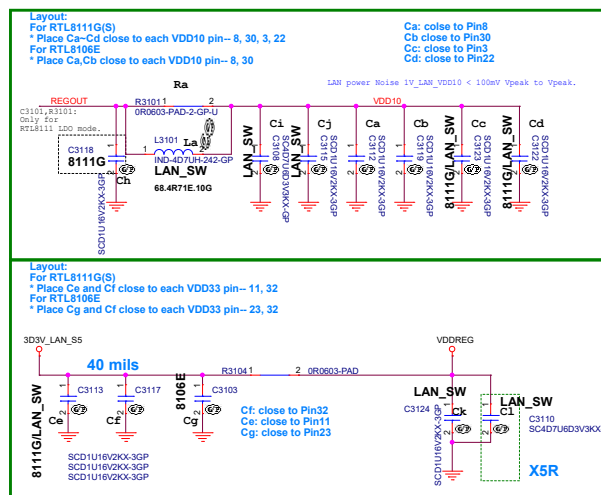
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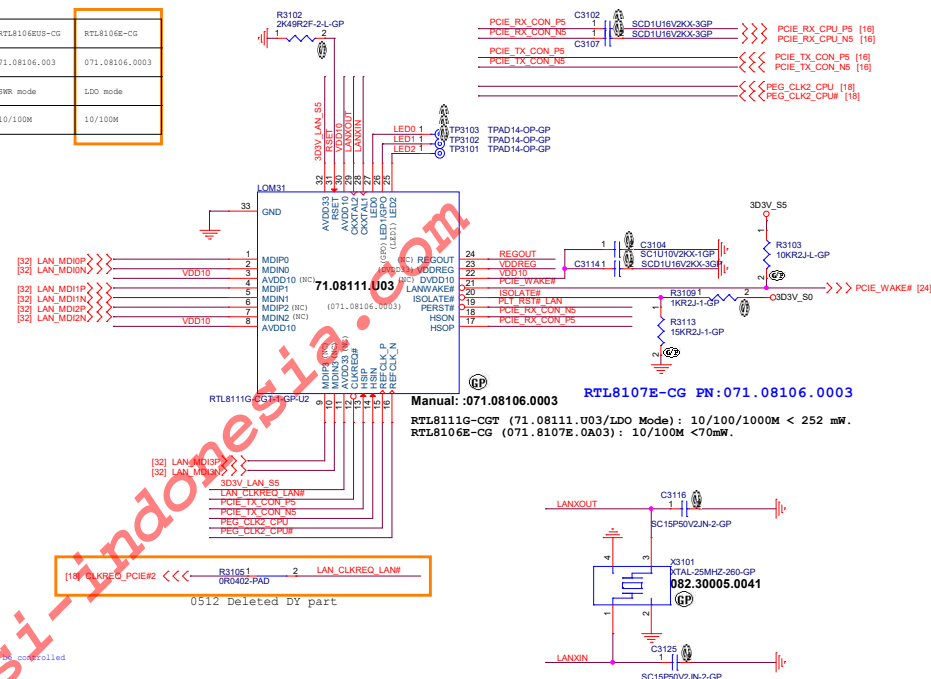
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Main Func = LAN



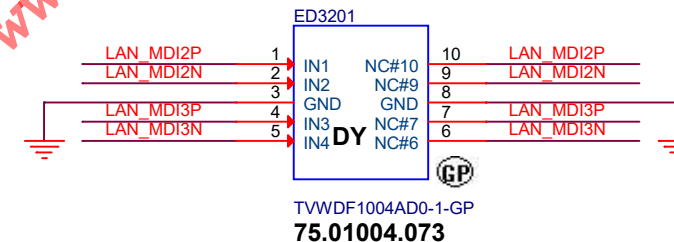
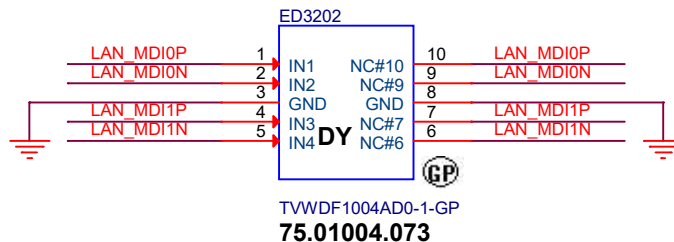
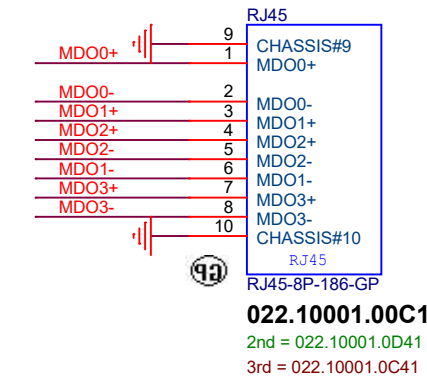
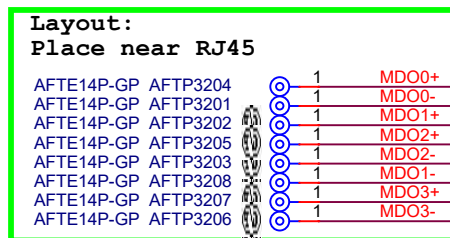
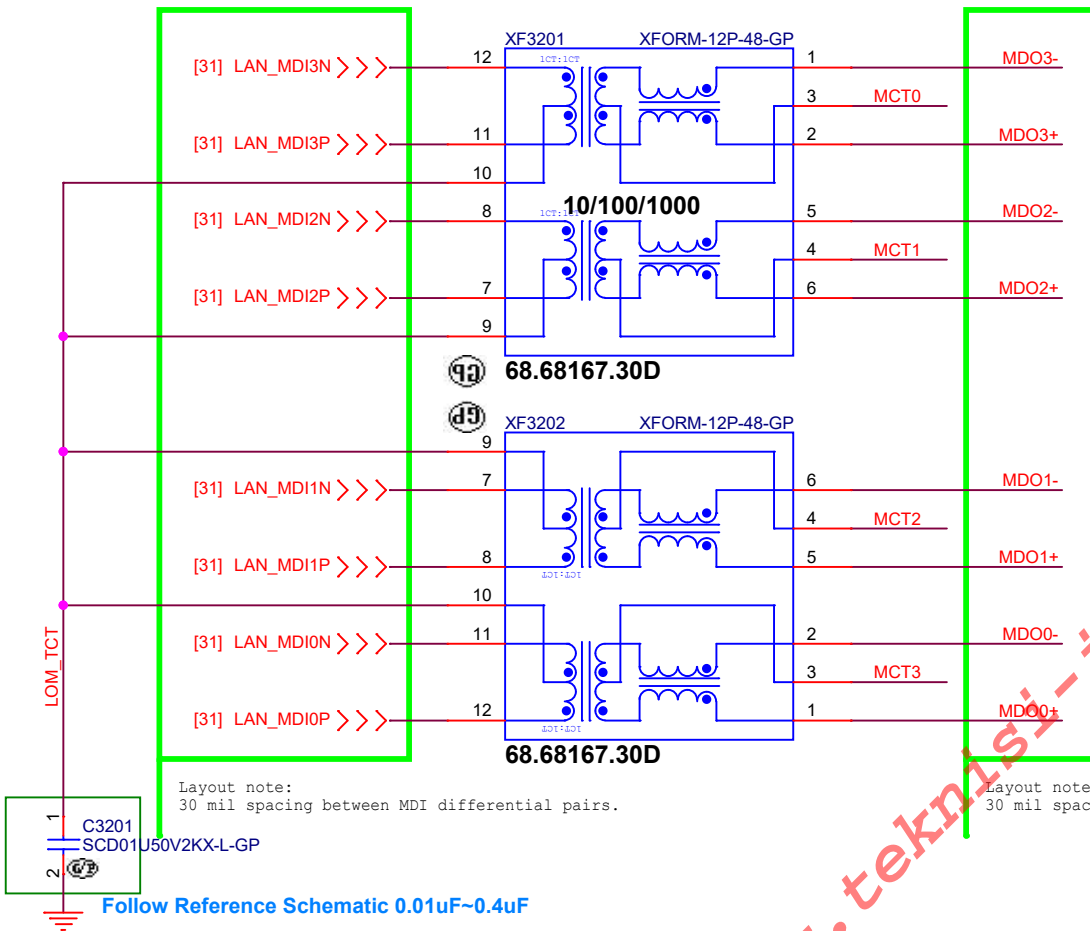
RTL8111GUS-CG	RTL8111G-CGT	RTL8106EUS-CG	RTL8106E-CG
71.08111.W03	71.08111.U03	71.08106.003	071.08106.0003
SWR mode	LDO mode	SWR mode	LDO mode
10/100/1000M	10/100/1000M	10/100M	10/100M

LAN CHIP (10/100/1000M & 10/100M co-lay)

[illegible]

Main Func = LAN

LAN TransFormer (10/100/1000M & 10/100M co-lay)



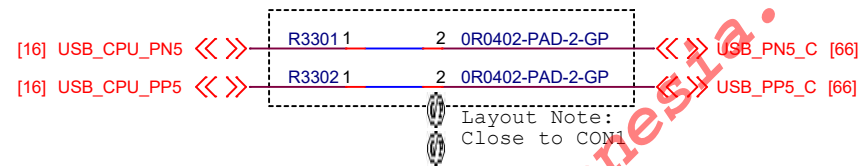
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DELL Wistron Corporation
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Title: **XFOM&RJ45**

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Main Func = Card Reader



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Title Card Reader-RTS5170			
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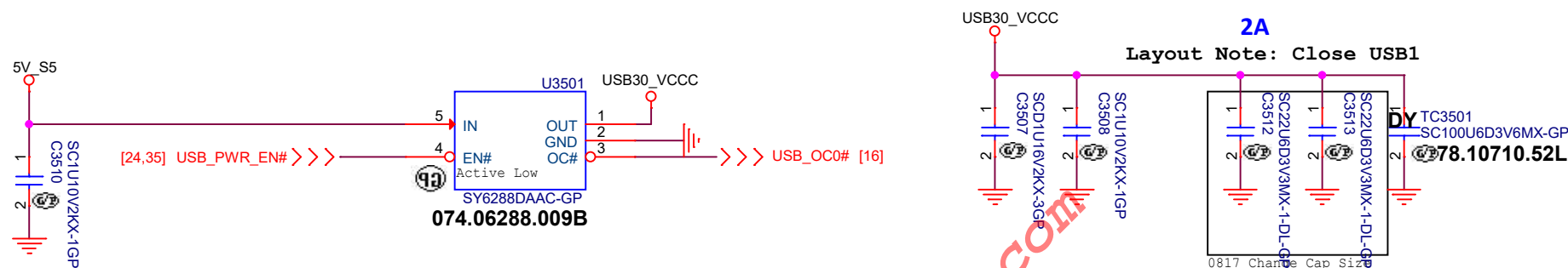
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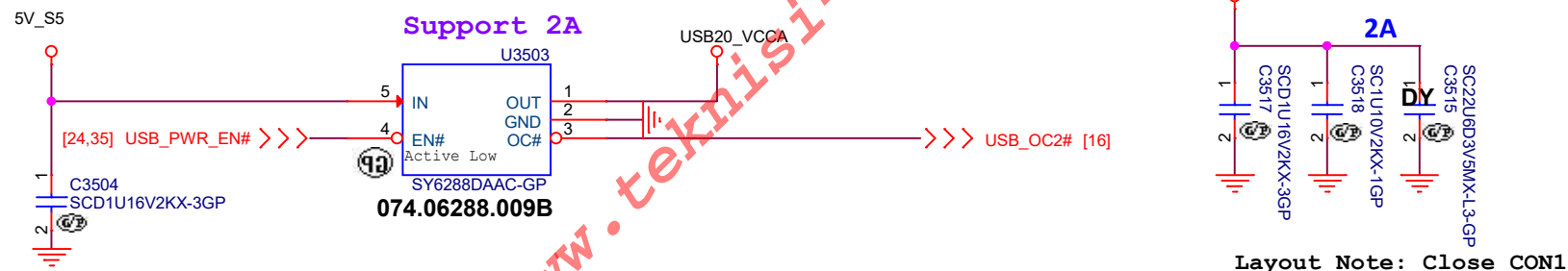
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Main Func = USB3.0 Port1



Main Func = USB2.0 Port3



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Title

USB switch

Size

Document Number

Turis/Vegas KBL-R

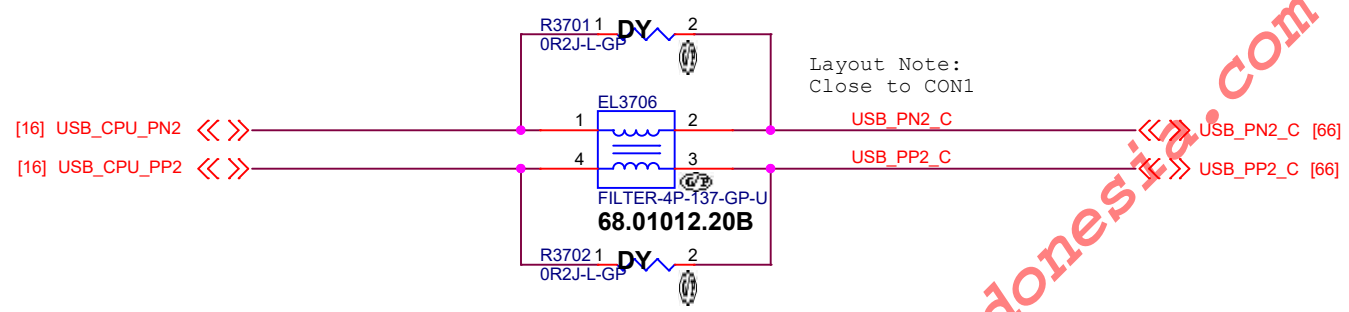
Rev

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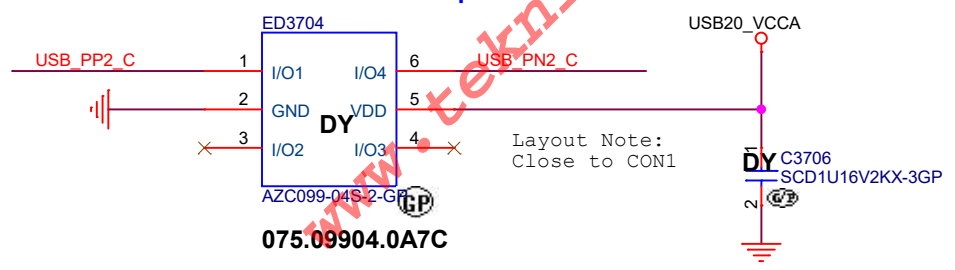
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USB port 3 (USB2.0 only) CMC



USB ESD Diode Stuff for ESD R2 spec




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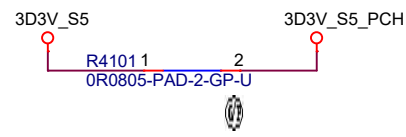
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Main Func = Power & Sequence



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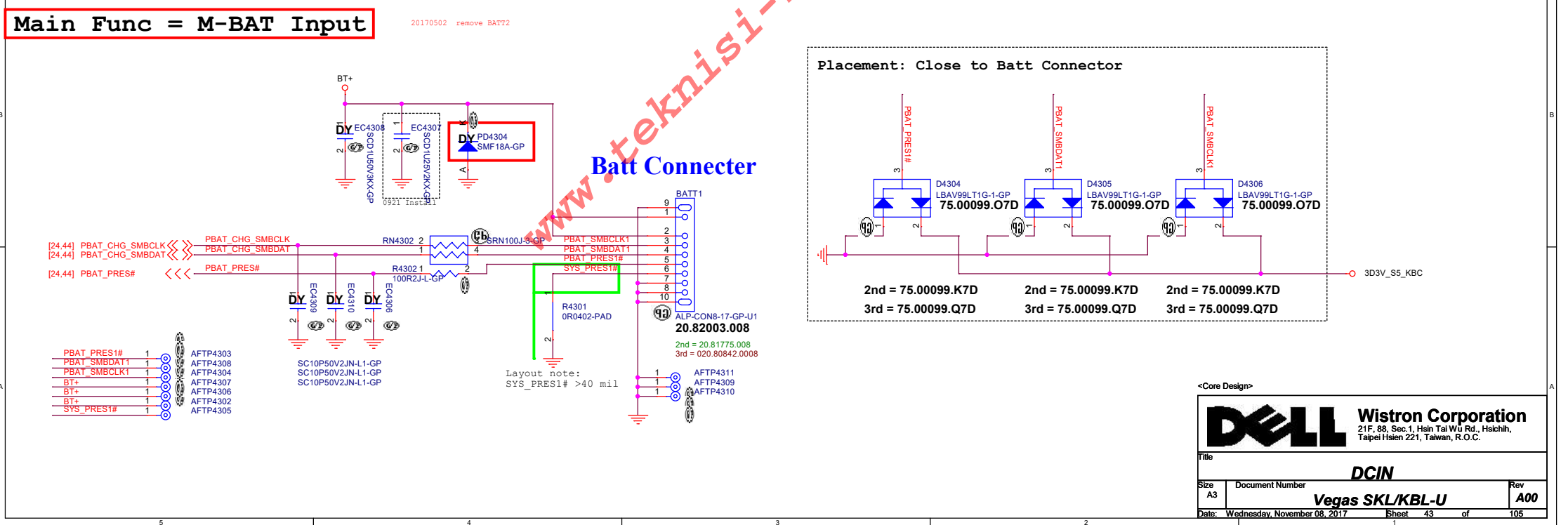
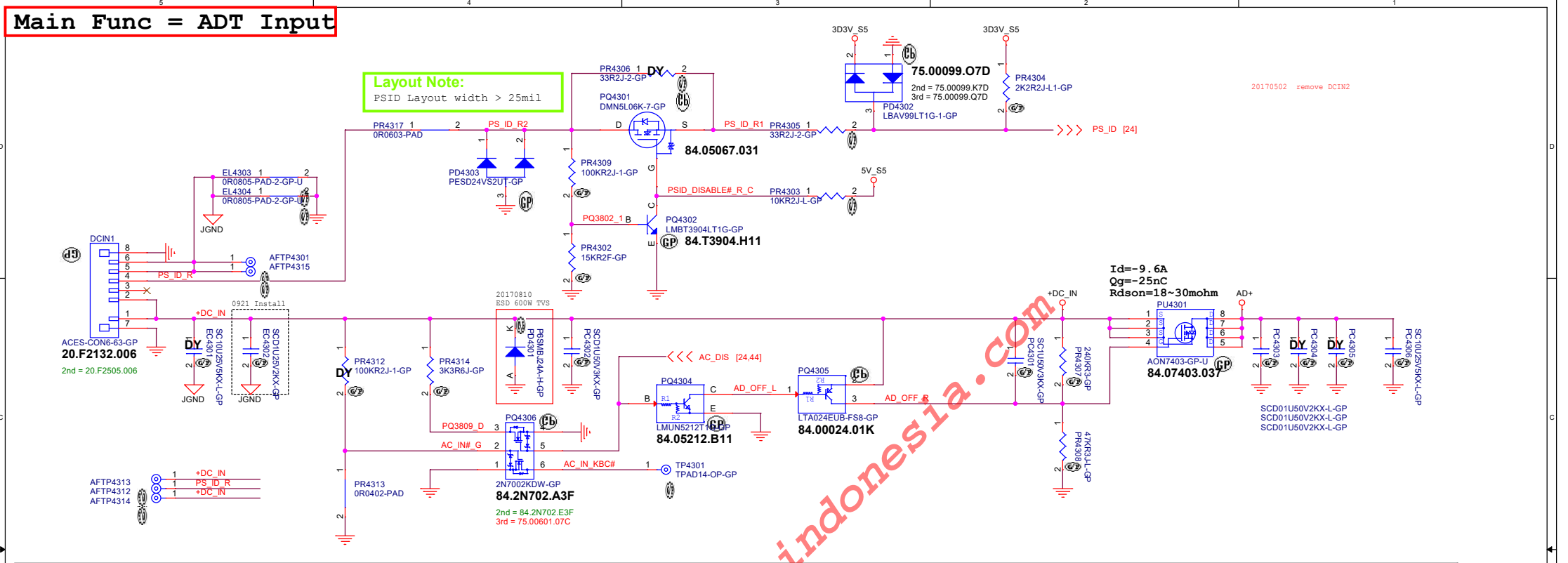
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Title Connected_Standby(1/2)+DS3		
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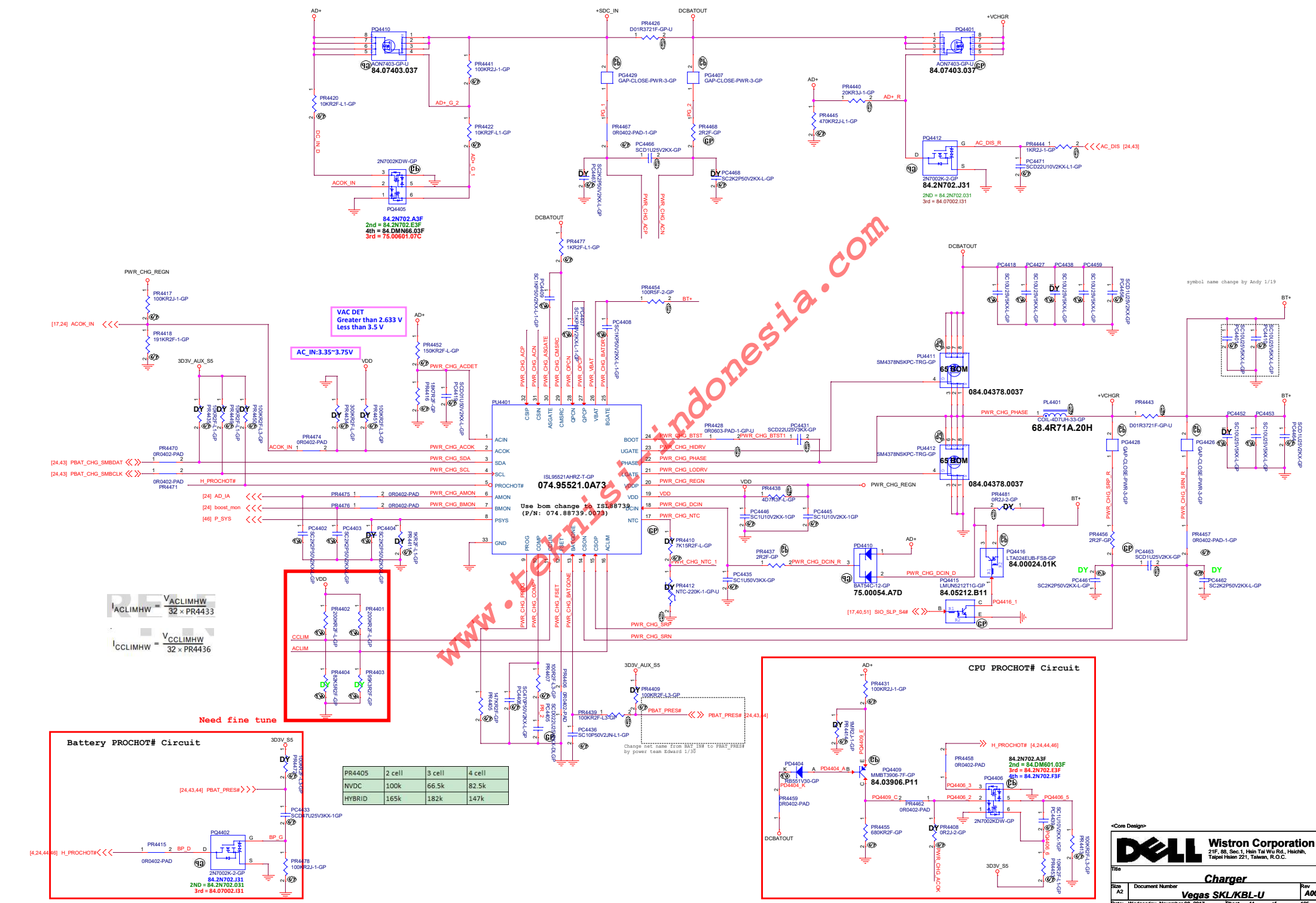
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<Core Design>

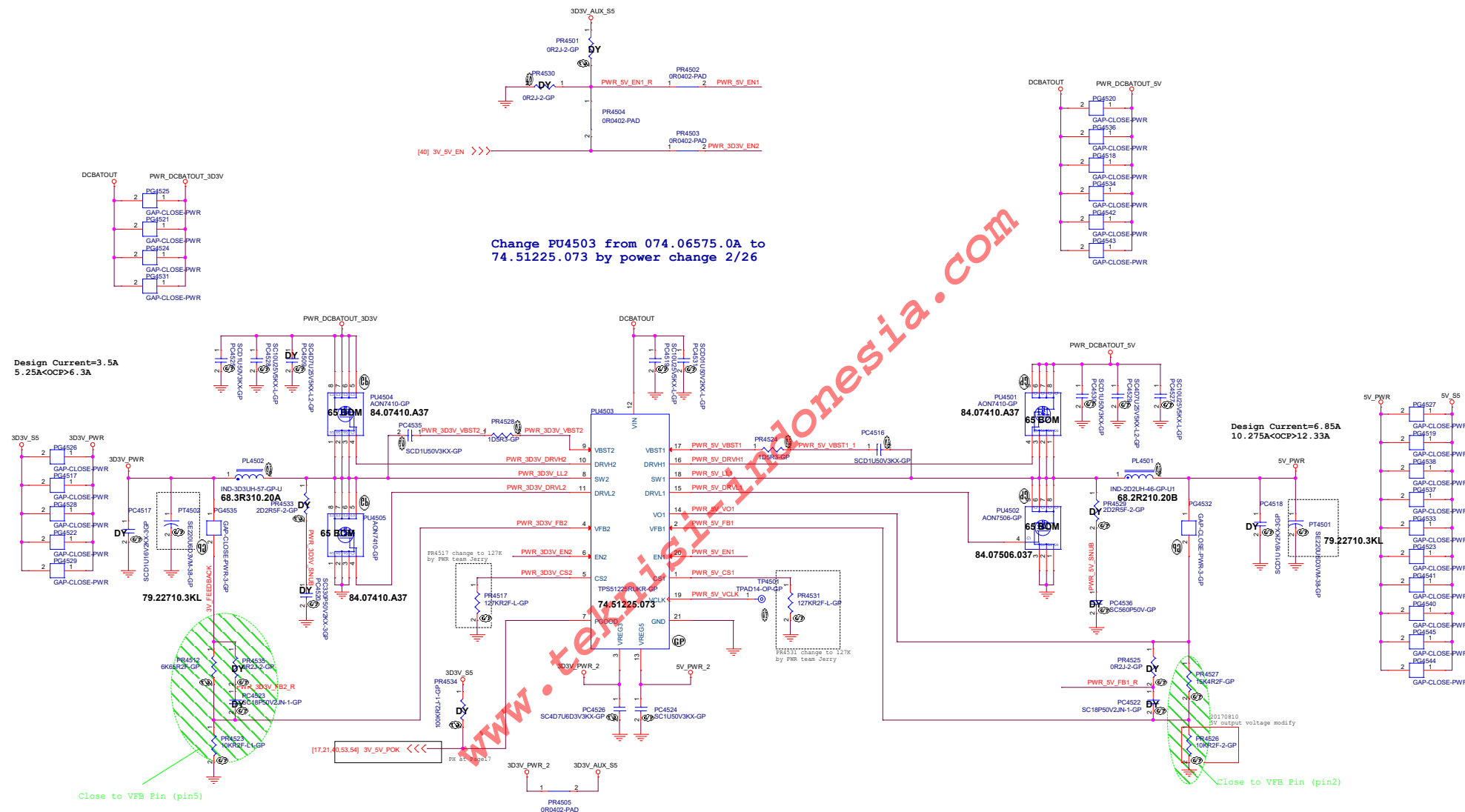
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Title Connected_Standby(2/2)			
Size A4	Document Number Vegas SKL/KBL-U		Rev A00
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Main Func = Charger



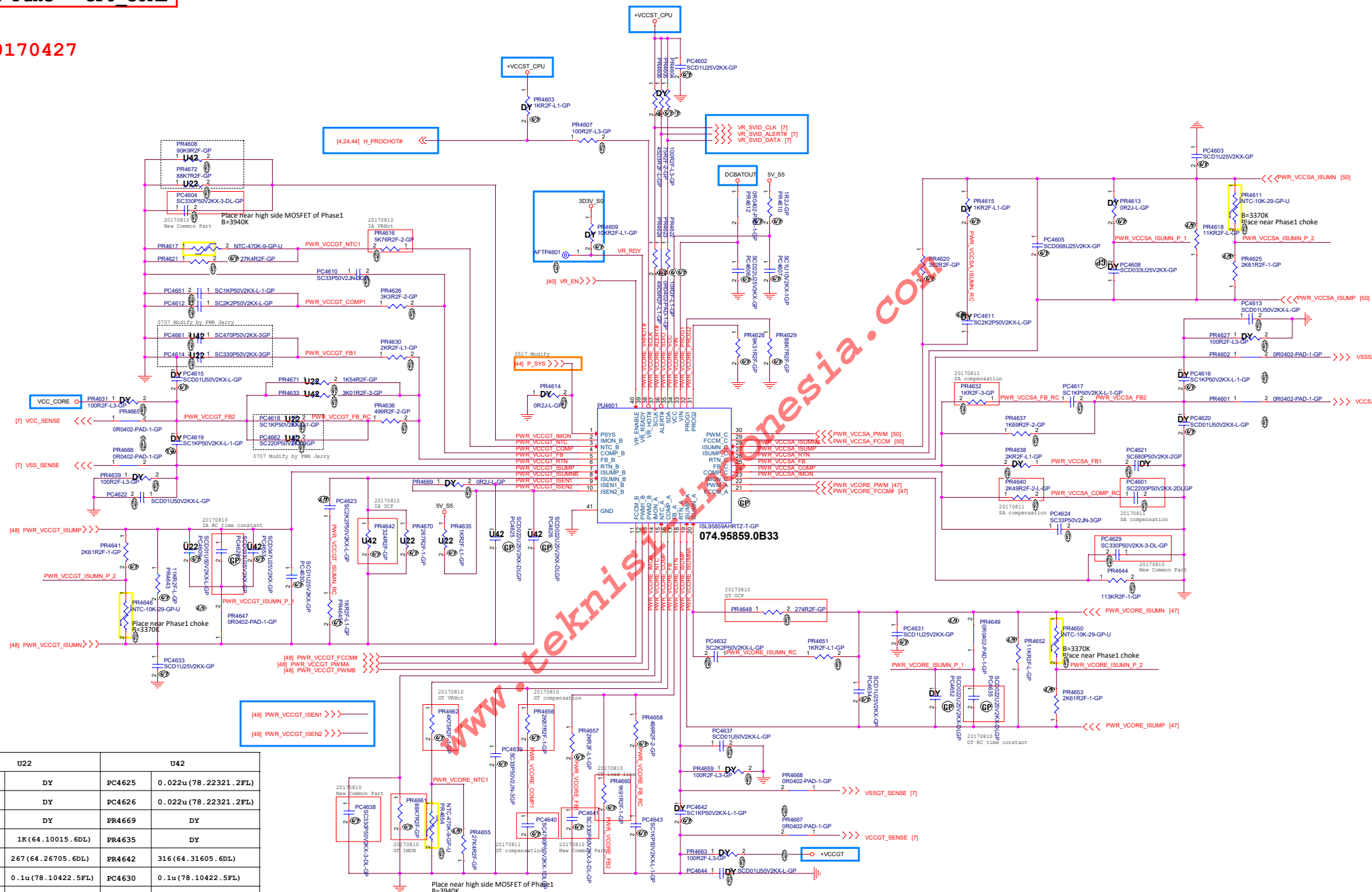
Main Func = 3D3V_5V



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cytotec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: CHIP CAP EL 220U 6.3V M6.3*4.4 /Chemi-con/ 18mohm / 79.22710.3KL
H/S: SIS412 / 24mohm/30mohm@4.5Vgs / 84.00412.037
L/S: SIS412 / 24mohm/30mohm@4.5Vgs / 84.00412.037

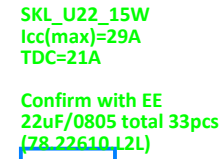
I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap: CHIP CAP EL 220U 6.3V M6.3*4.4 /Chemi-con/ 18mohm / 79.22710.3KL
H/S: SIS412 / 24mohm/30mohm@4.5Vgs / 84.00412.037
L/S: SIS780 / 14.5mohm/17.5mohm@4.5Vgs / 84.00780.037

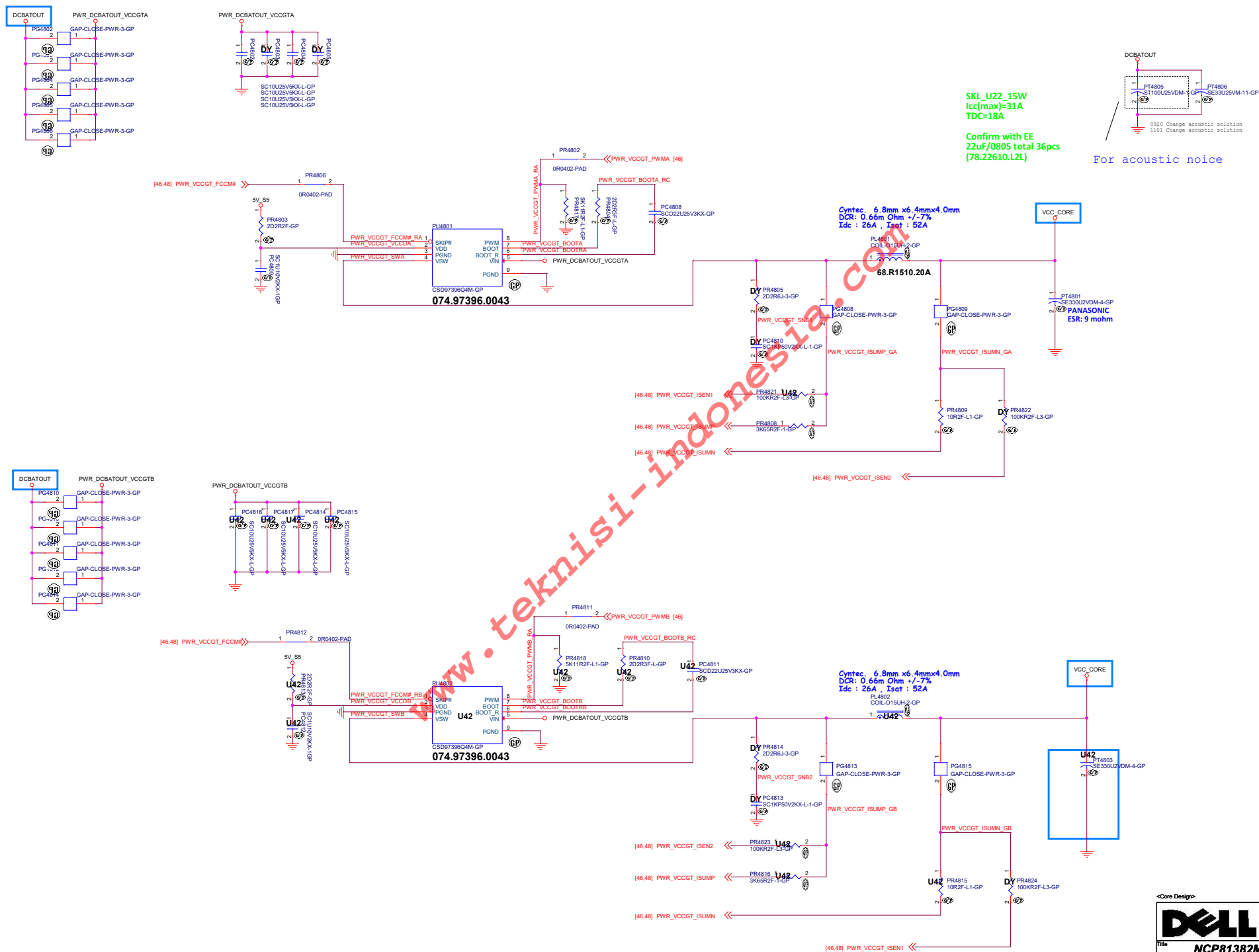
20170427



U22		U42	
PC4625	DY	PC4625	0.022u (78.22321.2FL)
PC4626	DY	PC4626	0.022u (78.22321.2FL)
PR4669	DY	PR4669	DY
PR4635	1K (64.10015.6DL)	PR4635	DY
PR4670	267 (64.26705.6DL)	PR4642	316 (64.31605.6DL)
PC4630	0.1u (78.10422.5FL)	PC4630	0.1u (78.10422.5FL)
PC4609	0.01u (78.10324.10L)	PC4628	0.022u (78.22322.2FL)
PC4653	DY	PC4653	47n (78.47322.2FL)
PR4671	1.54K (64.15415.6DL)	PR4633	3.01K (64.30115.6DL)
PR4672	88.7K (64.88725.6DL)	PR4608	90.9K (64.90925.6DL)
PC4614	330p (78.33124.2FL)	PC4661	470p (78.47124.2FL)
PC4618	1000p (78.10224.2FL)	PC4662	220p (78.22124.2FL)

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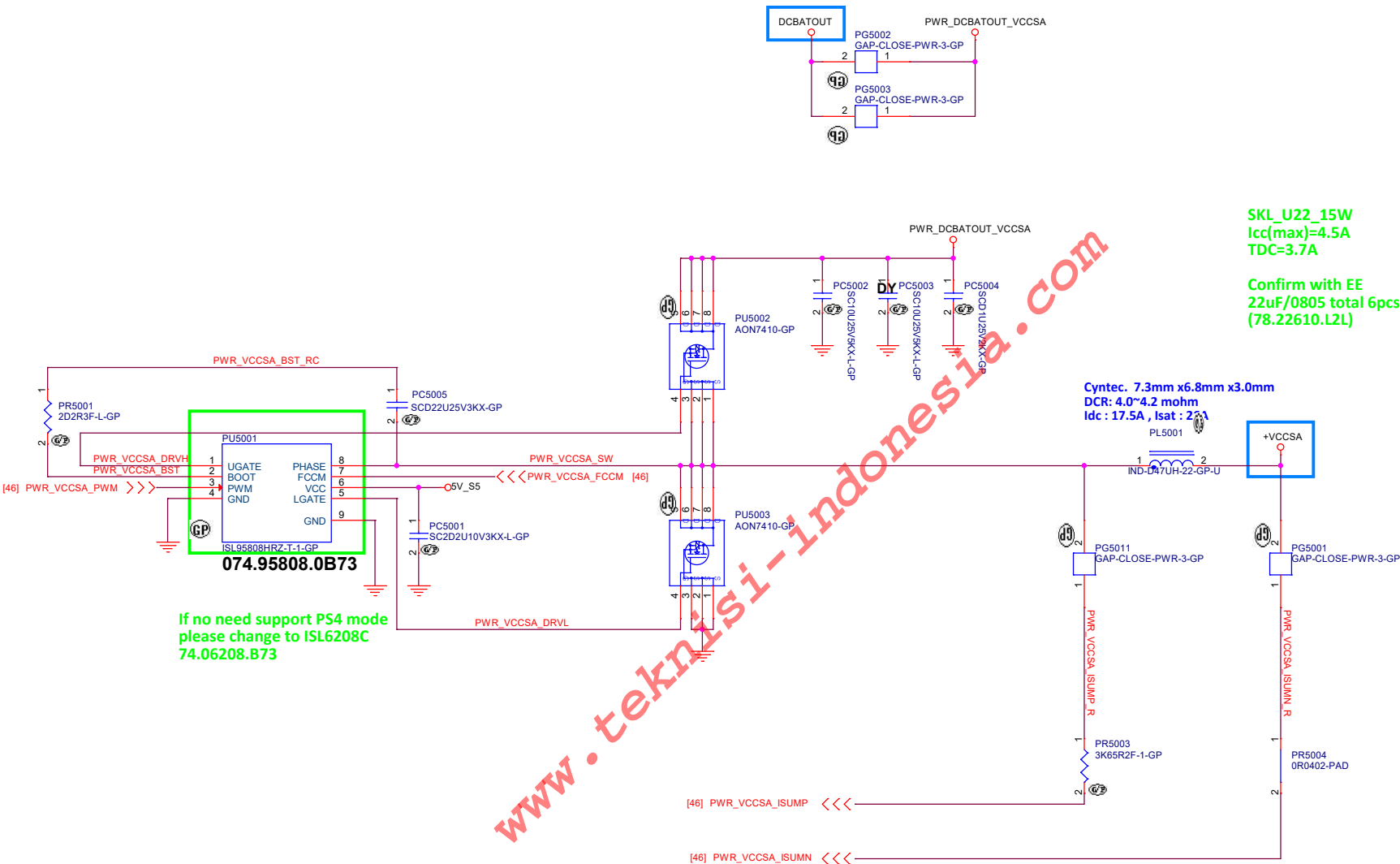
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Title			NCP81210MN_CPU_VCCGTUS		
Size	Document Number				Rev
A4	Vegas SKL/KBL-U				A00
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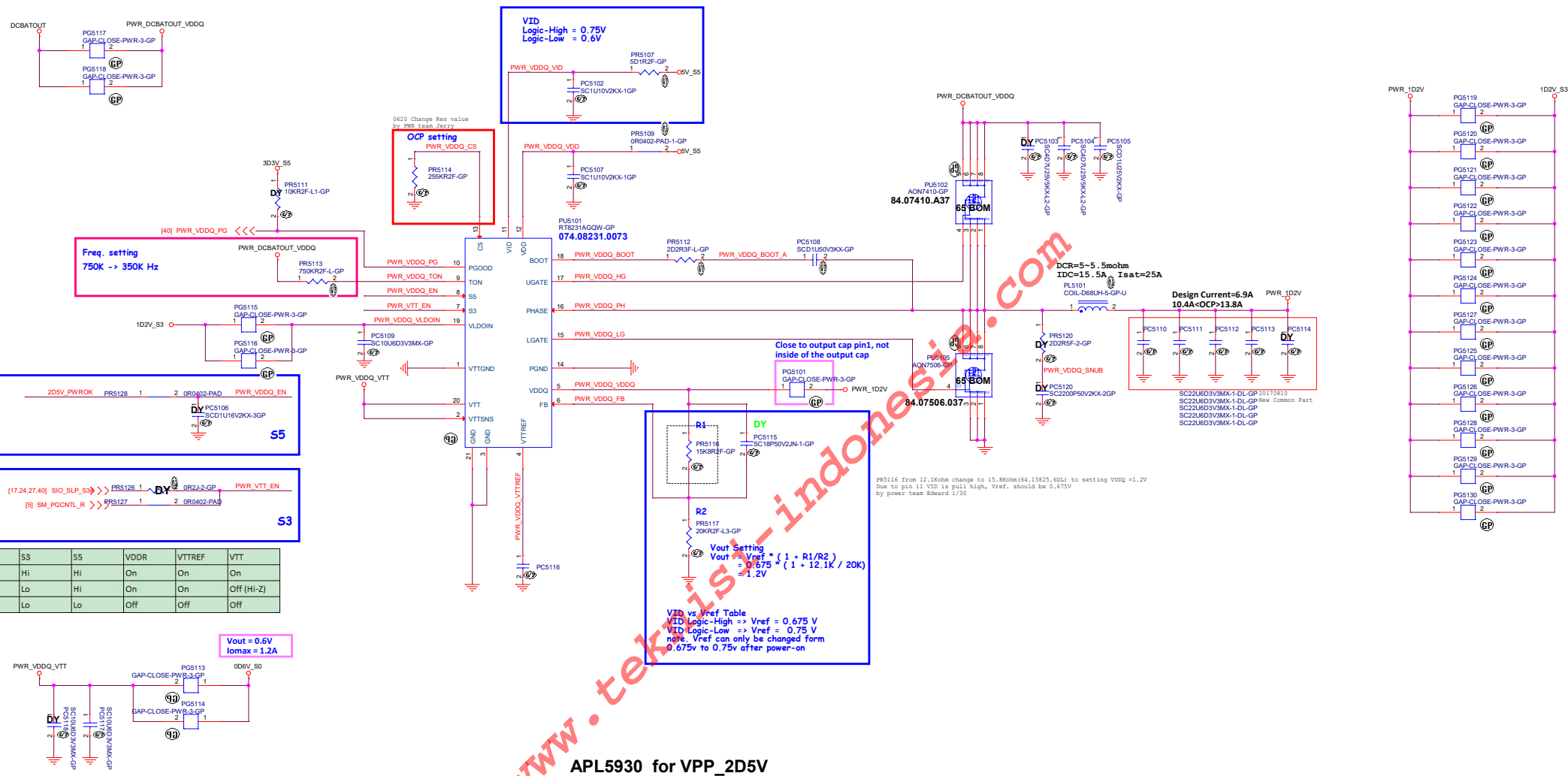
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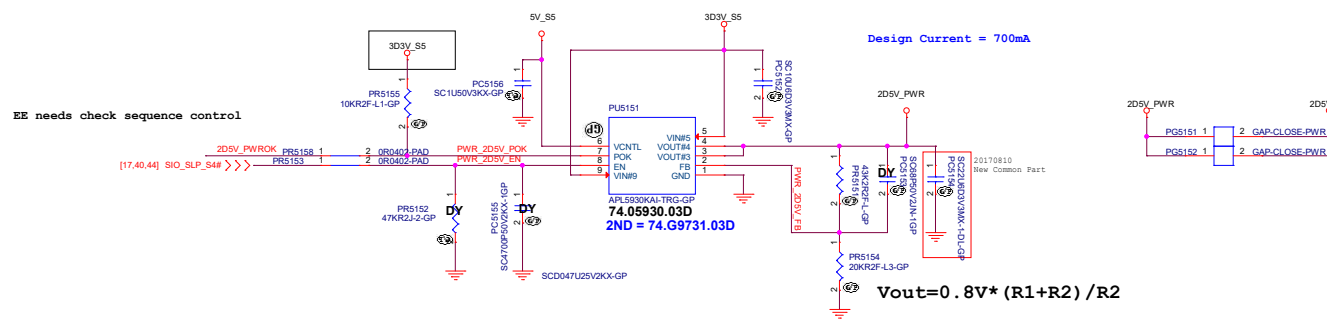
SKL_U22_15W
Icc(max)=4.5A
TDC=3.7A

Confirm with EE
22uF/0805 total 6pcs
(78.22610.L2L)

```
SSID = PWR.Plane.Regulator 1p2v& 2D5V
```



APL5930 for VPP_2D5V



Design Current = 700mA

$$V_{out} = 0.8V * (R1 + R2) / R2$$

(Blanking)

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Title

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Size
A4

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AOZ2262 for 1D0V

<Core Design>



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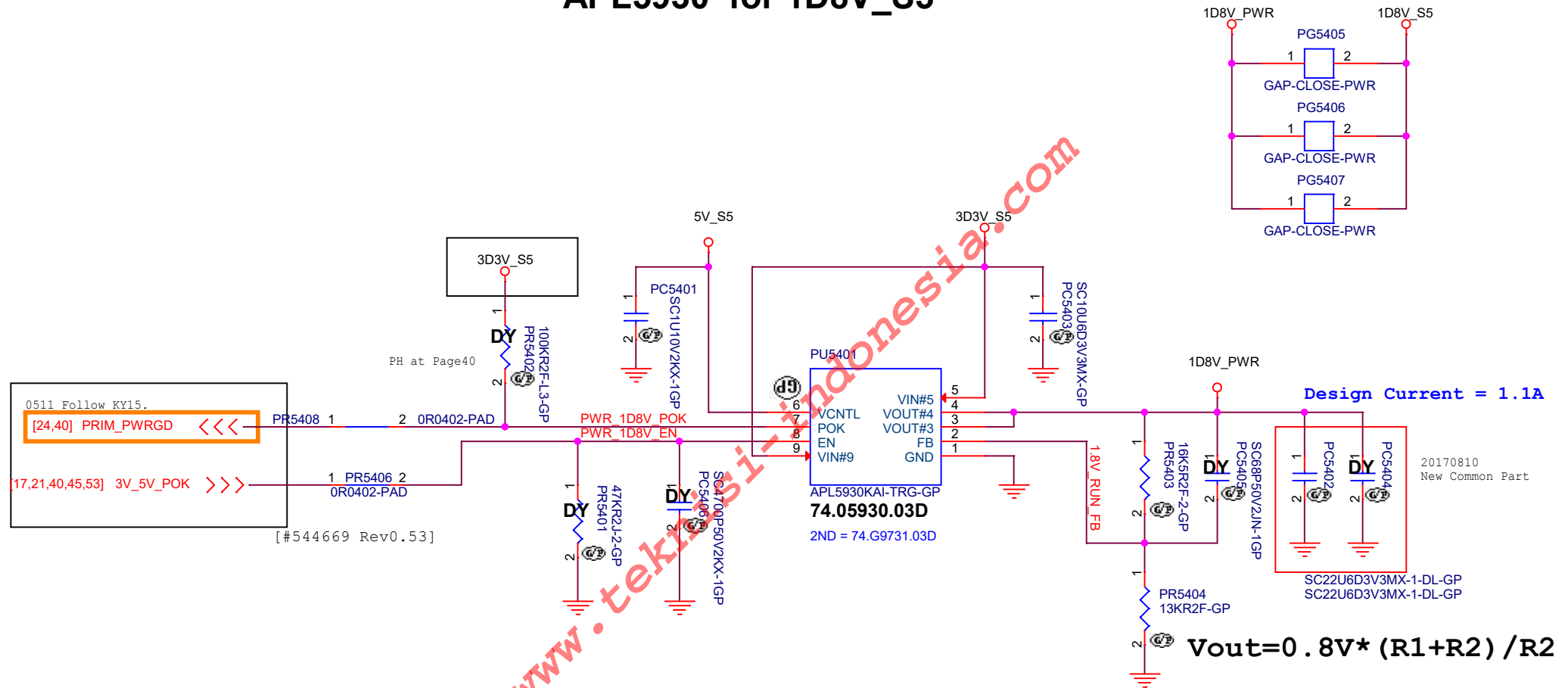
Size	Document Number
Custom	Vegas SKL/KBL-U

Rev	A00
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Main Func = 1D8V

APL5930 for 1D8V_S5



<Core Design>



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Title

LDO-V1D5V&V1D8V

Size
A4

Document Number

Vegas SKL/KBL-U

Rev
A00

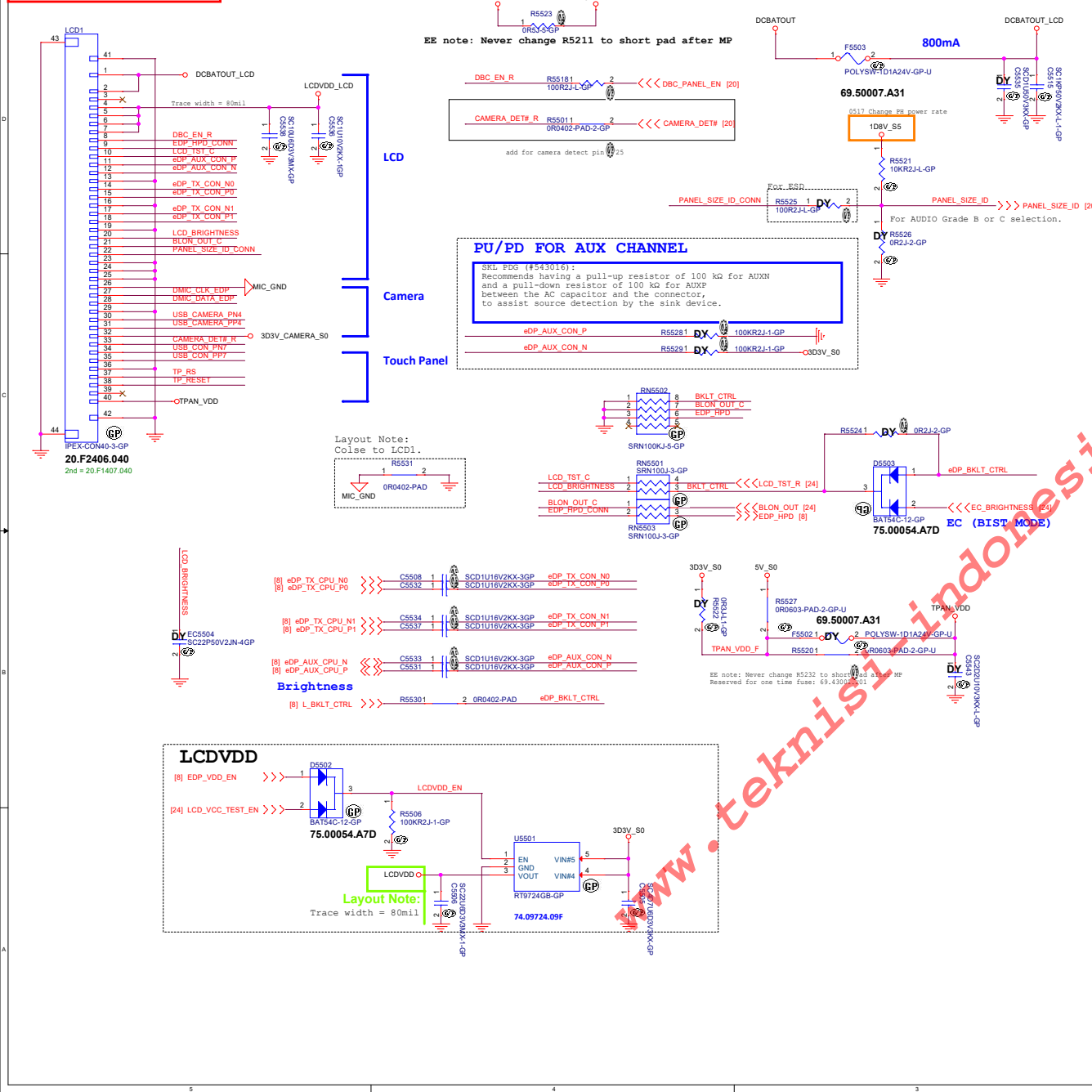
Date: Wednesday, November 08, 2017

Sheet 54

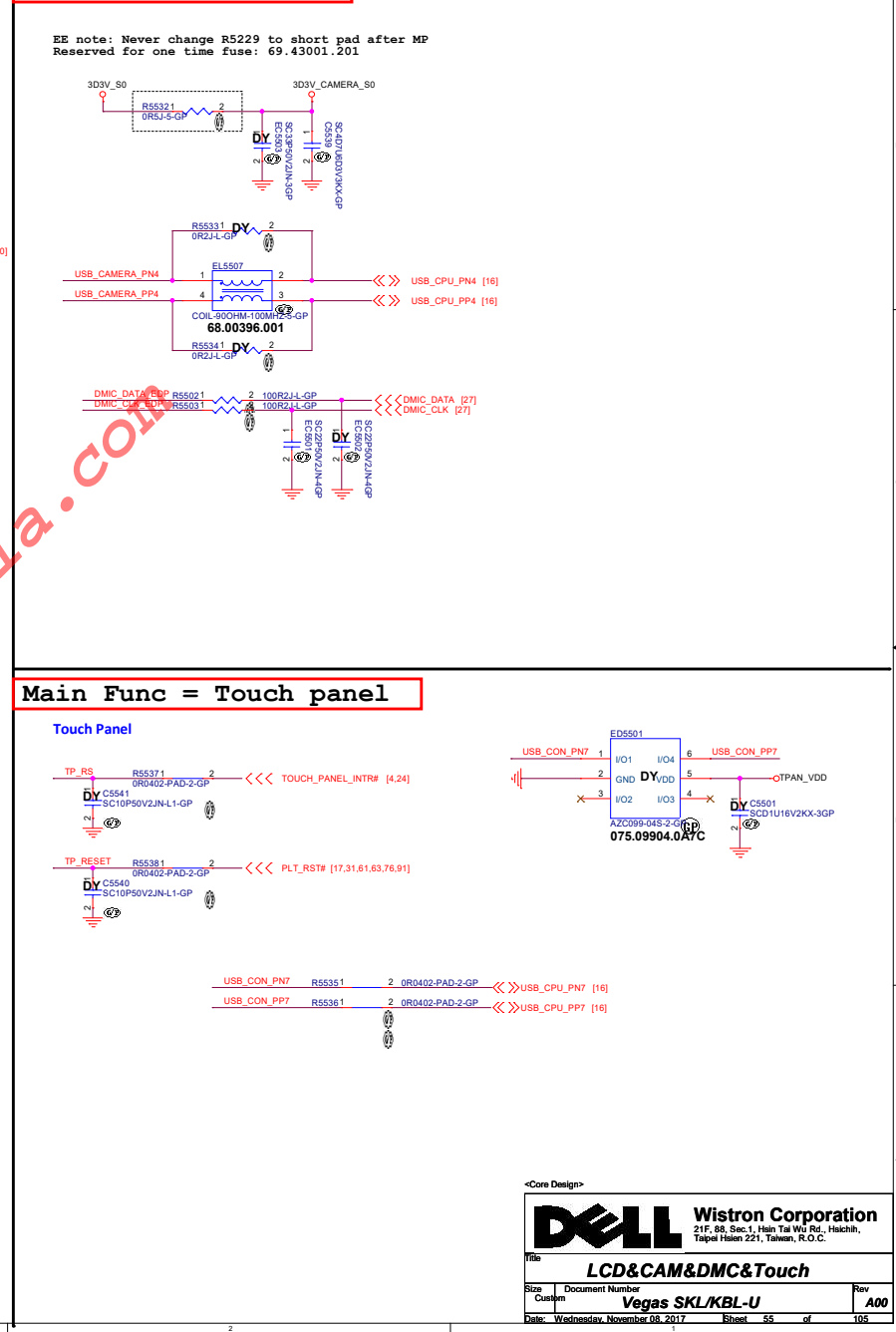
of

105

Main Func = LCD



Main Func = CAMERA






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Title (Blanking)			
Size A4A4	Document Number Vega 941 841/MBL-U		Rev A00
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Title

Display (RSVD)

Size
A4

Document Number

Vegas SKL/KBL-U

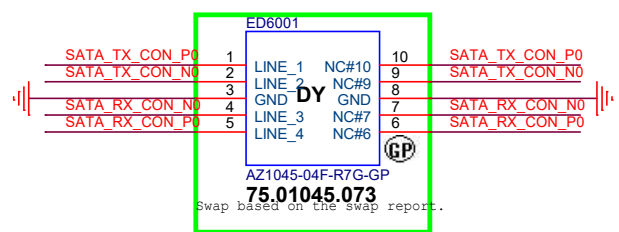
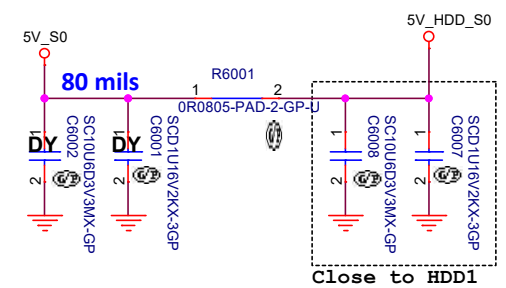
Rev
A00

Date: Wednesday, November 08, 2017

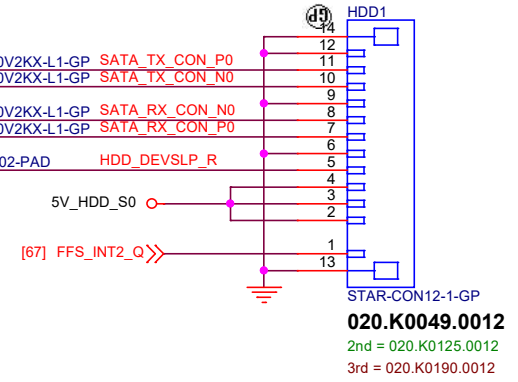
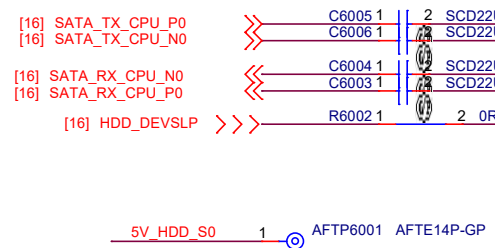
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Main Func = HDD

SATA HDD Connector



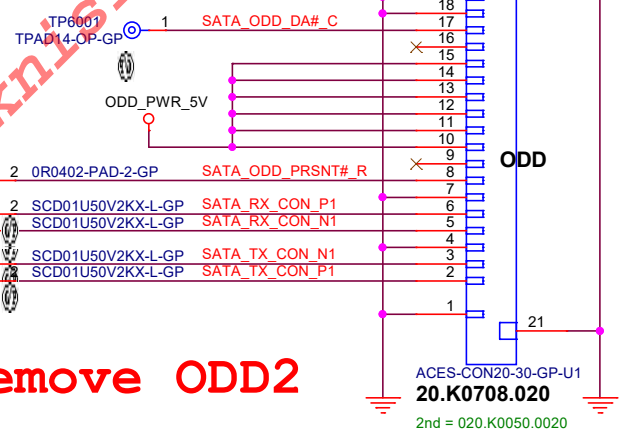
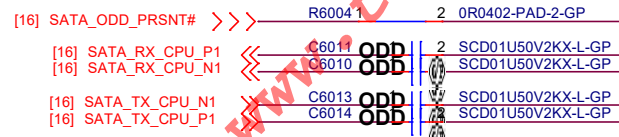
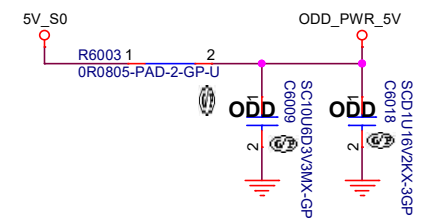
Layout Note:
Place near HDD1



CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
GND	P1	
GND	P2	
GND	P3	
5V	P4	10
5V	P5	11
5V	P6	12
GND	P7	
GND	P8	

Main Func = ODD

ODD Connector



20170502 remove ODD2

<Core Design>

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Title
INT IO (HDD/ODD)

Size
Custom

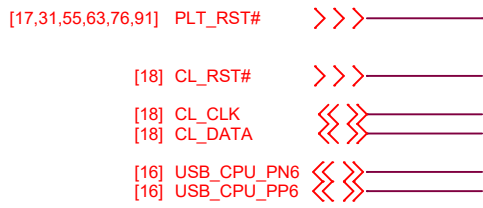
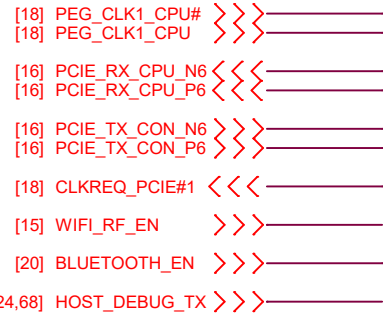
Document Number
Vegas SKL/KBL-U

Rev
A00

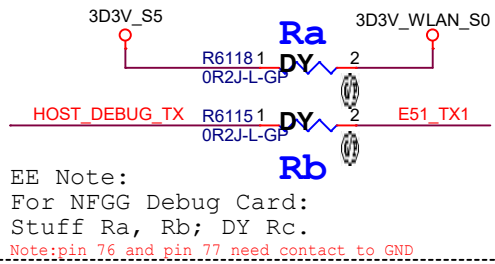
Date: Wednesday, November 08, 2017

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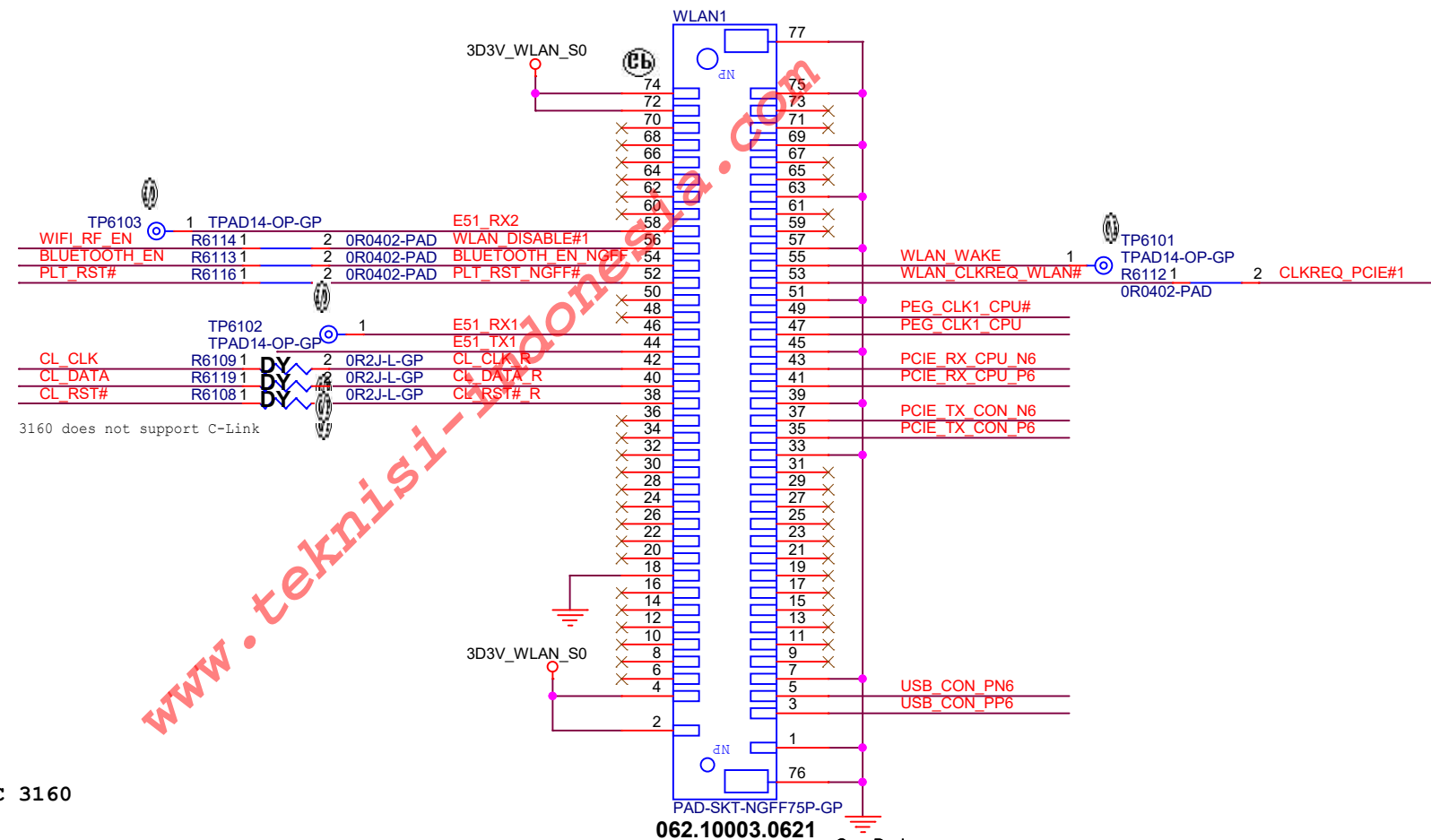
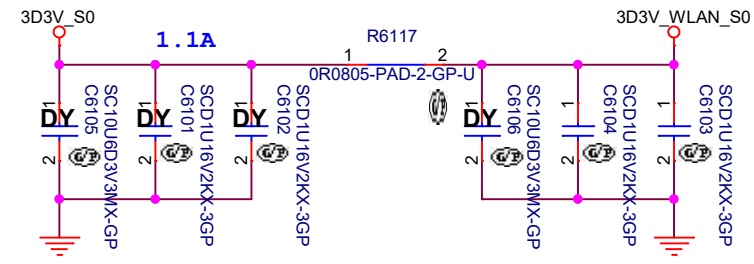
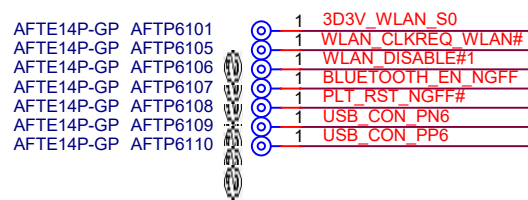
Main Func = WLAN



Reserved for NGFF Debug Card



Support: Intel Dual Band Wireless-AC 3160



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Title
NGFF WLAN CONN


Size A4 Document Number
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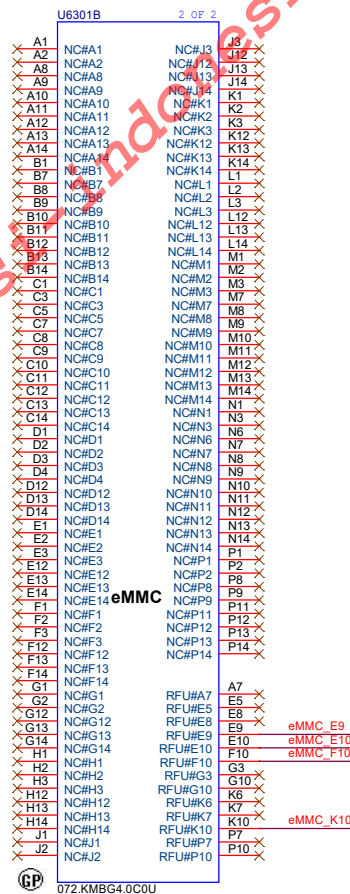
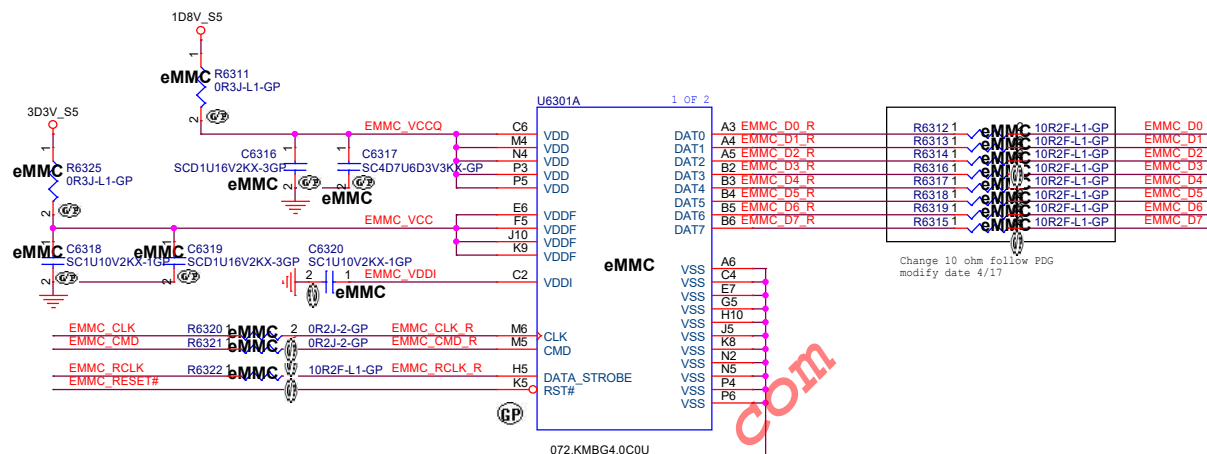
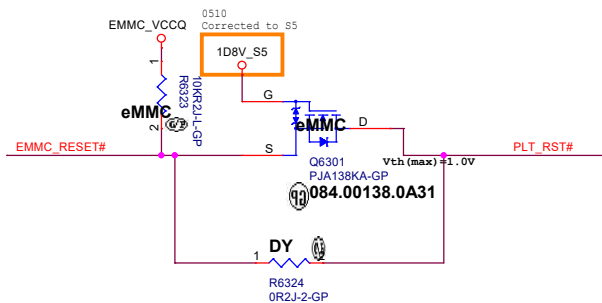
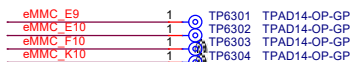
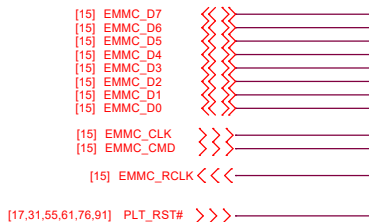
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Title			
Reserved			
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Main Func = eMMC

EMMC

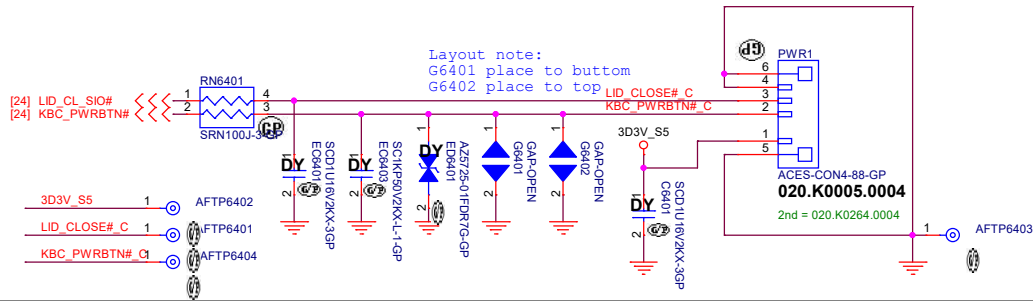


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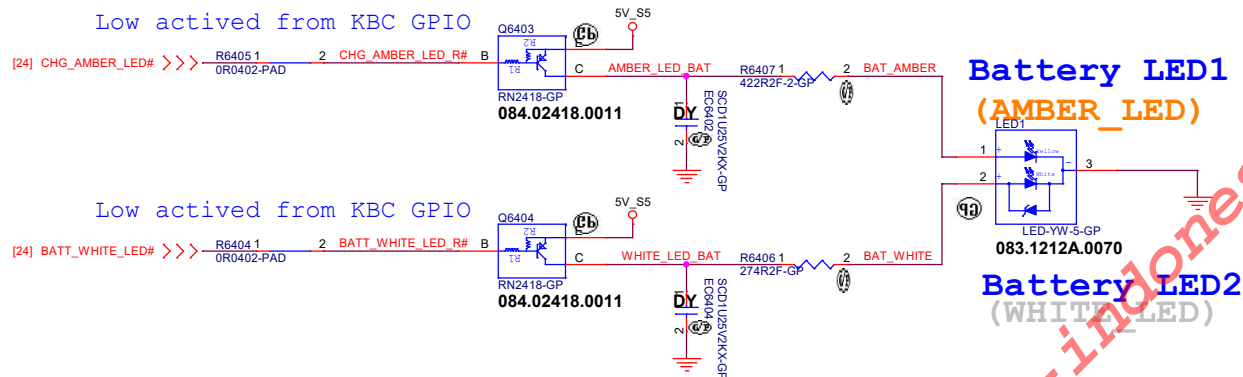


Title			eMMC
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Power button

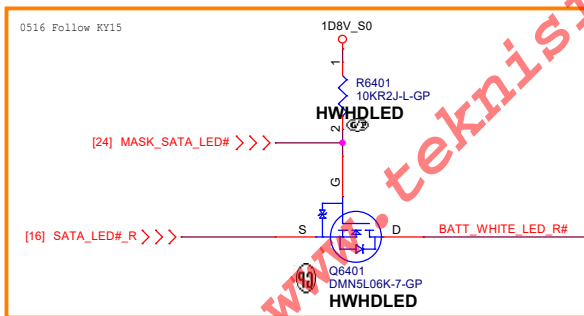


Main Func = Battery LED



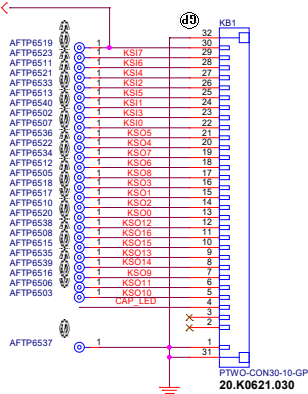
Main Func = HDD LED

SATA HDD LED LOW actived from PCH GPIO



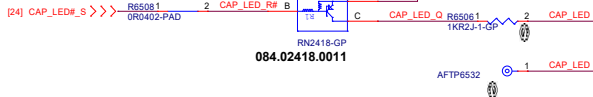
Main Func = KB

Internal Keyboard Connector



CAP LED Control

LOW acted from KBC GPIO



0502 Deleted KB2
0524 Deleted KBBL1 block

Main Func = TPAD

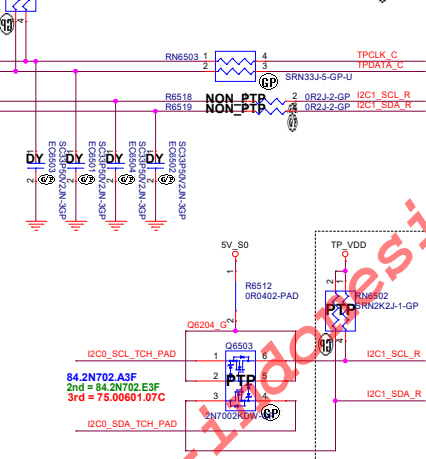
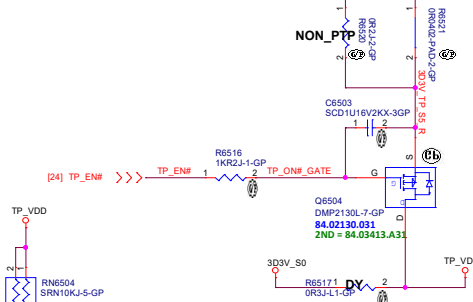
Support PTP

PS2

[24] CLK_TP_SIO <<<<
[24] DAT_TP_SIO <<<<

I2C

[20] I2C0_SCL_TCH_PAD >>>>
[20] I2C0_SDA_TCH_PAD <<<<

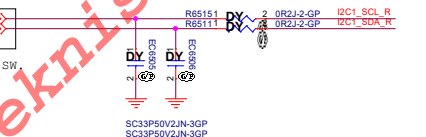


Vages install Non PTP

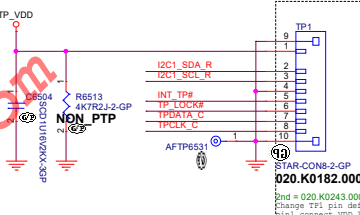
SMBUS

[12,13,18,56,67] PCH_SMBCLK <<<<
[12,13,18,56,67] PCH_SMBDATA <<<<

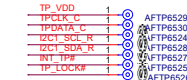
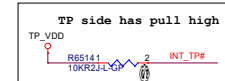
Need to check with SW



Precision Touch Pad Connector



Need to check if it is Active High or Active Low and check if there is PH on TPAD side.



Pin number	Pin name
1	VDD
2	DAT (I2C)
3	CLK (I2C)
4	GND
5	ATTN
6	GPIO
7	DAT (PS2)
8	CLK (PS2)

<Core Design>

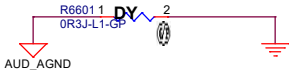
I/O Board Connector

Cardreader
USB3(USB2.0)

[33] USB_PN5_C
[33] USB_PP5_C
[37] USB_PN2_C
[37] USB_PP2_C

Universal Jack

[29] AUD_PORTA_L_R_B
[29] AUD_PORTA_R_R_B
[29] SLEEVE_R
[29] RING2_R
[29] JACK_PLUG



Pitch: 1mm
Power: 6 pins
GND: 7 pins
AGND: 2 Pins



<Core Design>

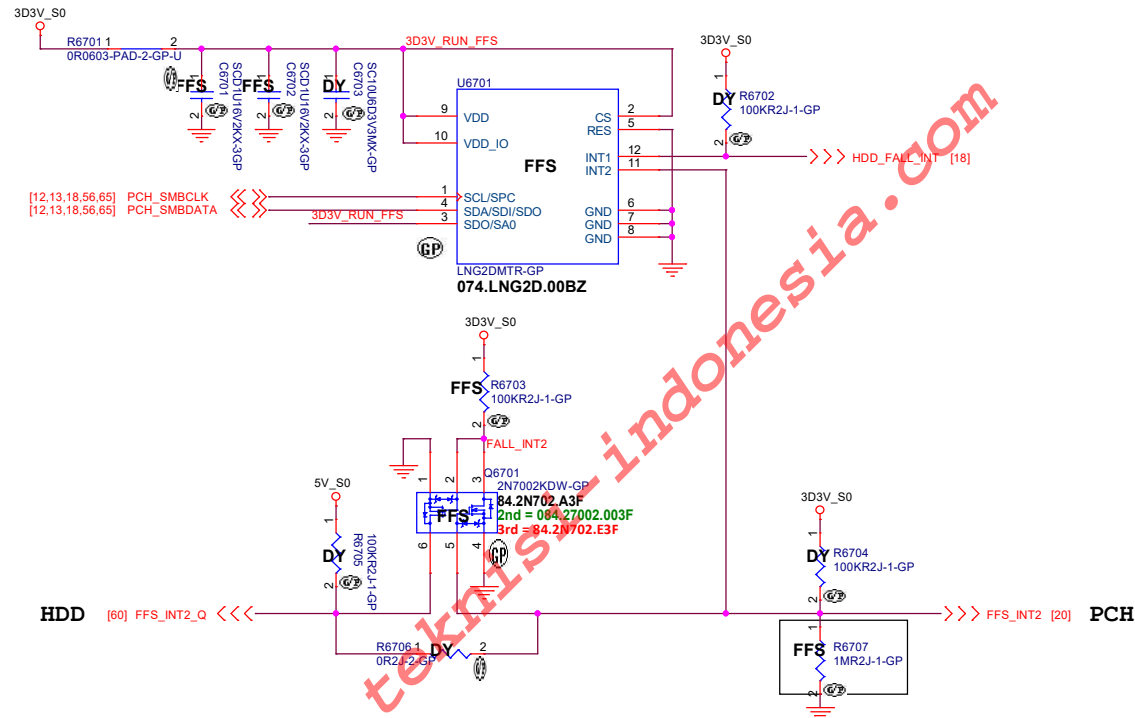
DELL Wistron Corporation
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Title			IO Board Connector		
Size	Document Number				Rev
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SSID = User.interface

Free Fall Sensor

DVT1 add FFS 2/18



Note

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

Note

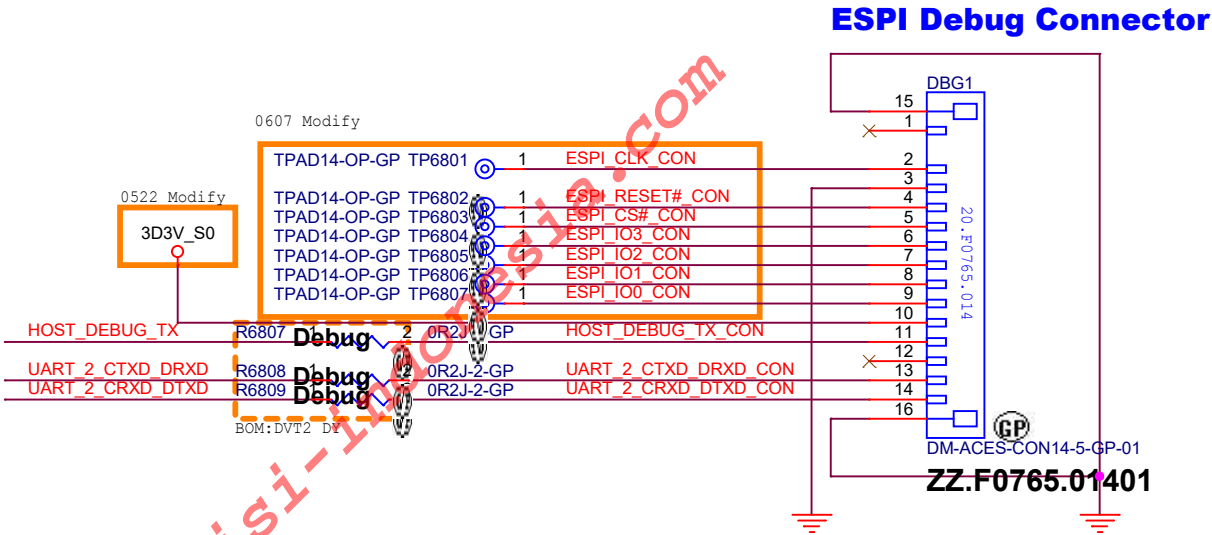
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

<Core Design>

Main Func = Debug

UART

[24,61] HOST_DEBUG_TX >>>
[20] UART_2_CTXD_DRXD >>>
[20] UART_2_CRXD_DTXD <<<



<Core Design>

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Title Dubug connector			
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Size A4	Document Number Vegas SKL/KBL-U		Rev A00
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Size
A4

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Title			
USB3.0 PORT			
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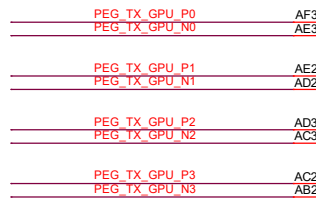
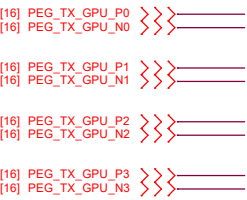
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Title			
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20170502



GFX & GPP, 85Ω
GFX & GPP CLK, 85Ω
GPU1A 1 OF 7

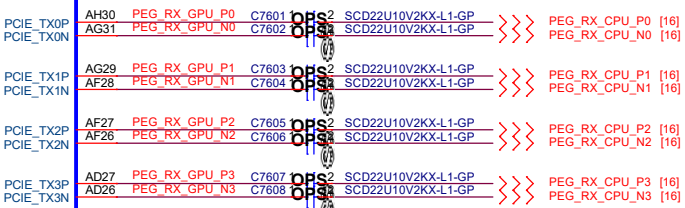
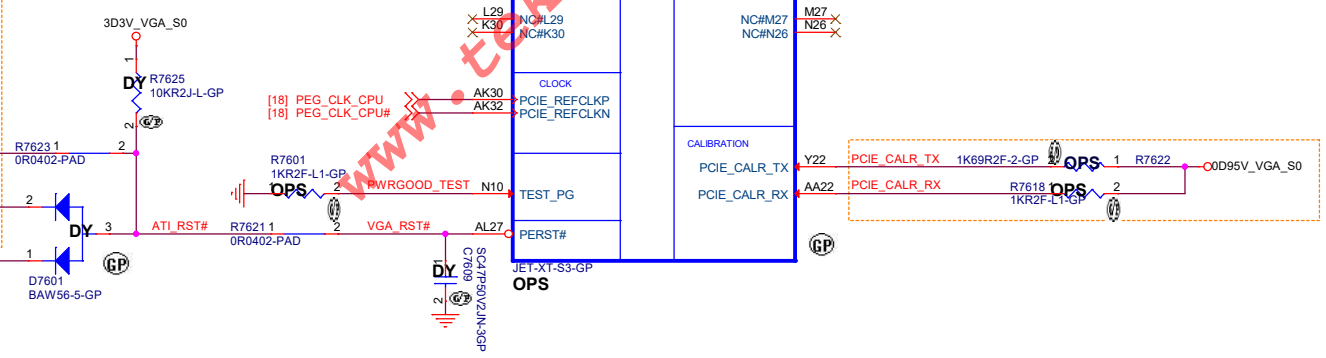
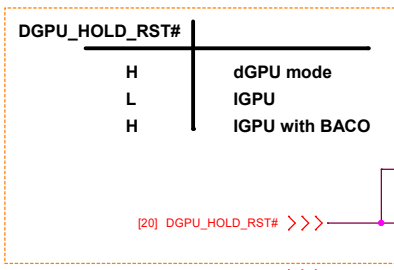


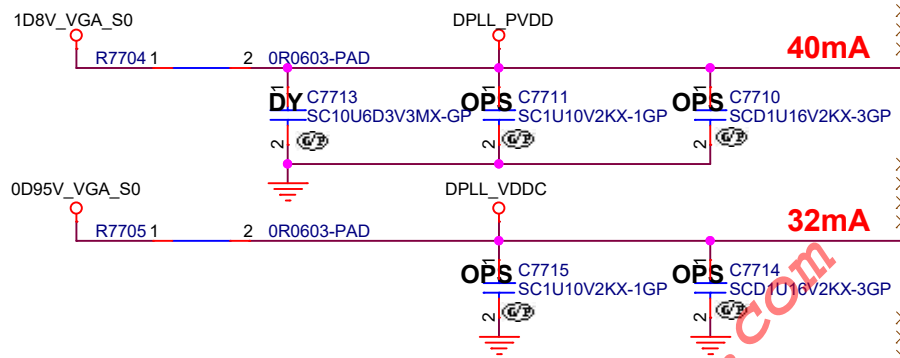
Table 3-5 PCI Express® Bus Interface

Pin Name	I/O	Description
PERSTb	I	Fundamental reset. 3.3-V tolerant pad. This signal must be asserted during any fundamental reset event, such as power up, warm boot, reset button pressed, CTL-ALT-DEL, Windows restart, or wake from D3.
PCIE_REFCLKP/N	I	PCI Express PLL differential reference clock (+/-). 100-MHz (± 300 ppm) input frequency; 0-V to 0.7-V single-ended swing.
PCIE_TX[7:0]P/N	O	PCI Express transmitter output data channel TX[7:0] (+/-). Differential serial data transmitted up to a 8.0-GT/s bit rate.
PCIE_RX[7:0]P/N	I	PCI Express receiver input data channel RX[7:0] (+/-). Differential serial data received up to a 8.0-GT/s bit rate.
PCIE_CALR_RX	I	Connect to PCIE_VDDC through a 1-kΩ (1% tolerance) resistor.
PCIE_CALR_TX	I	Connect to PCIE_VDDC through a 1.69-kΩ (1% tolerance) resistor.
CLKREQB	O	Reserved, do not connect on the PCB.

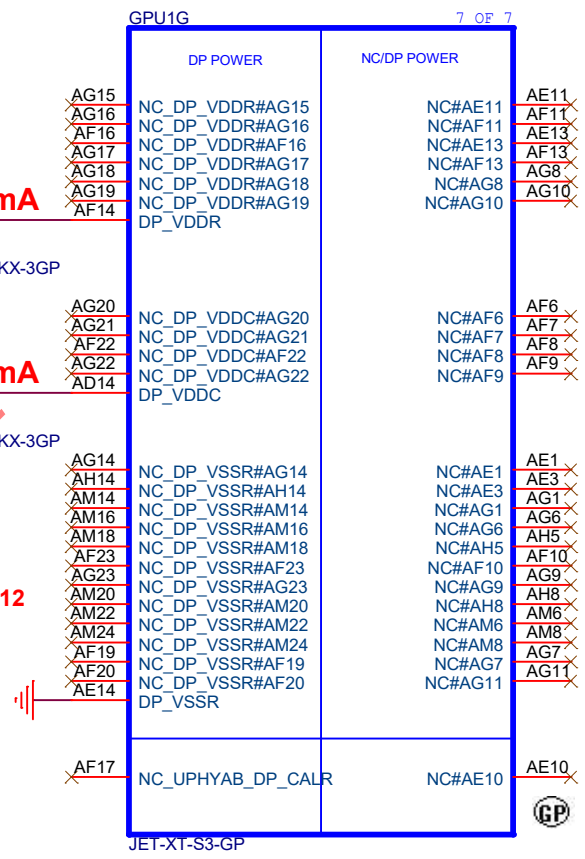
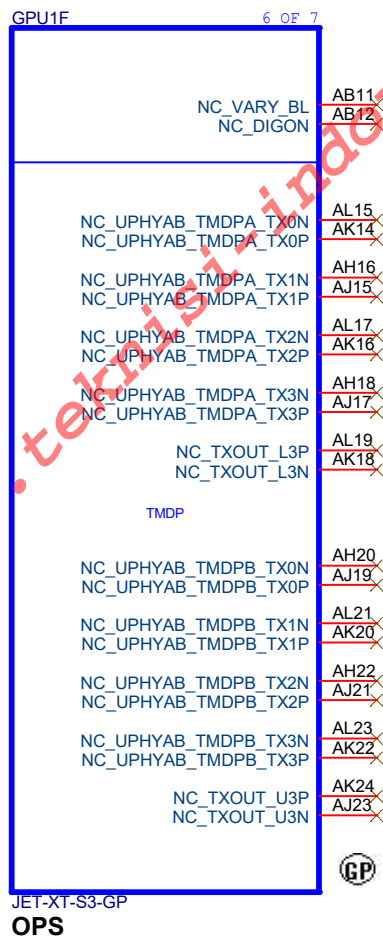
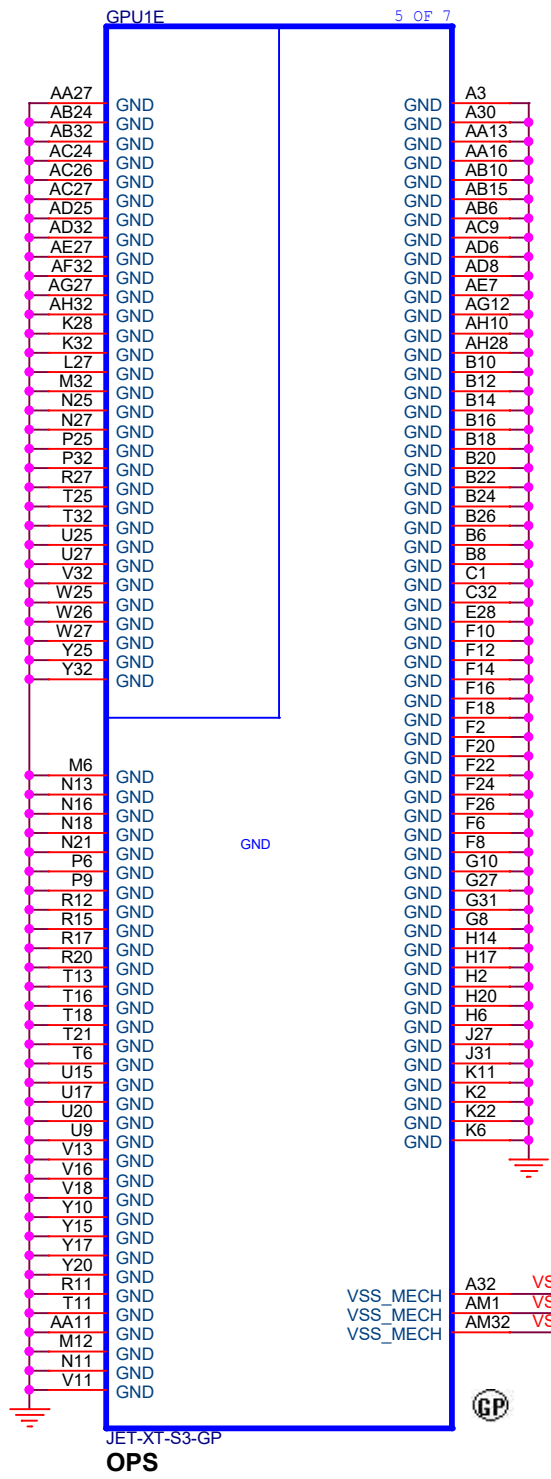


Main Func = dGPU

1.8V and 0.95V for Clock resource

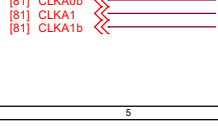
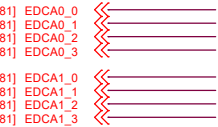
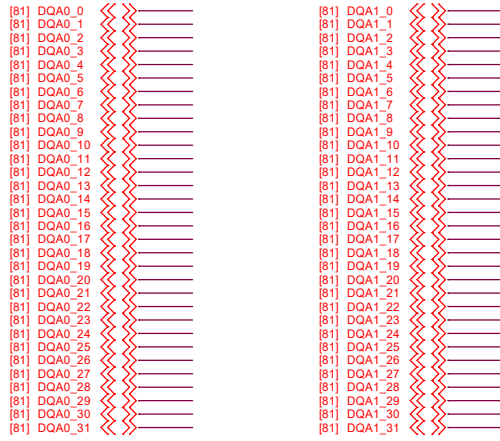


BALL: AB11, AB12
R16: NC
MESO: VDDC



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Title 077_GPU (2/5) DIGITALOUT			
Size	Project Name Vegas SKL/KBL-U		Rev x00
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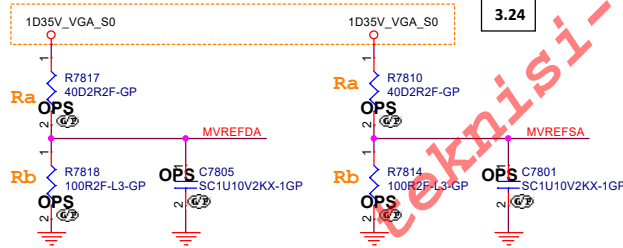
Main Func = dGPU



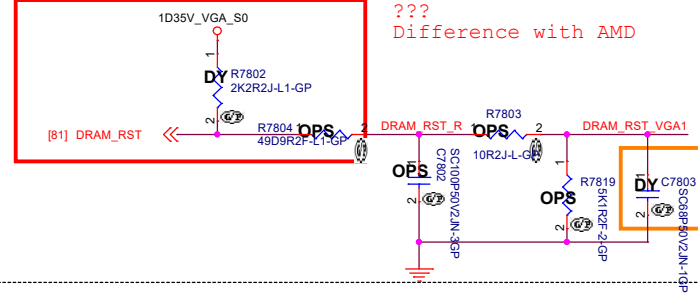
Please MVREF drivers and Caps close to ASIC

DDR3/GDDR3 Memory Stuff Option(R16)

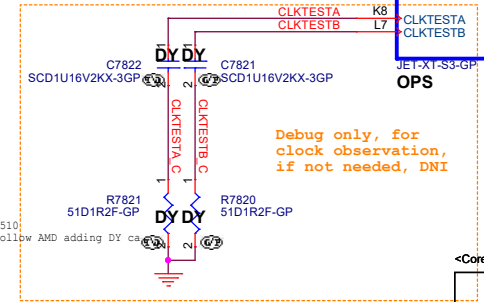
	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1D35V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R



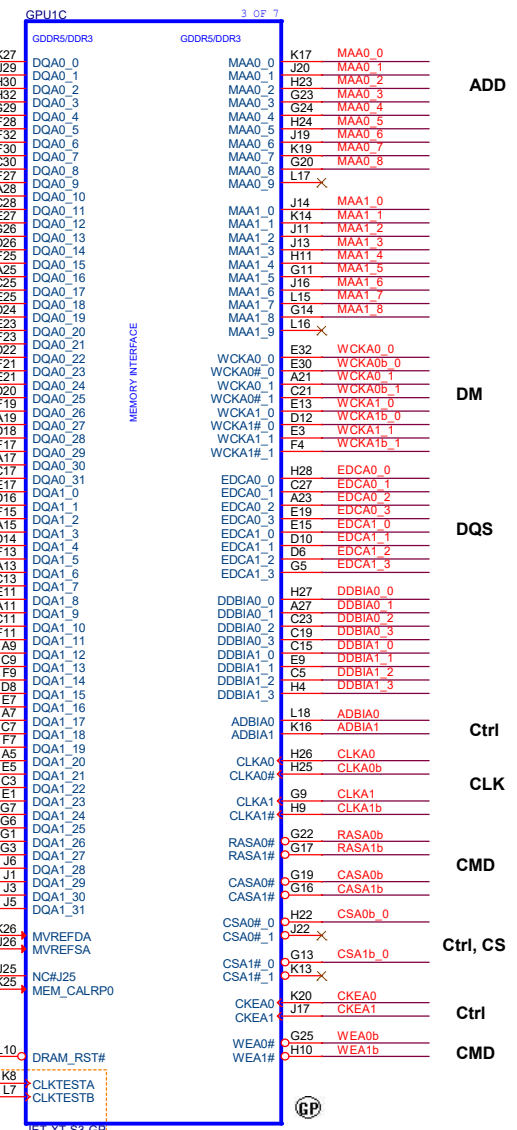
Place all these componets very close to GPU (within 25mm) and keep all componets close to each other
This basic topology should be used for DRAM_RST for DDR3/GDDR5

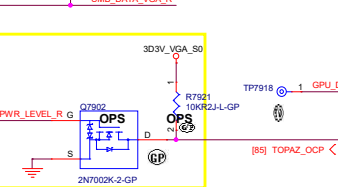
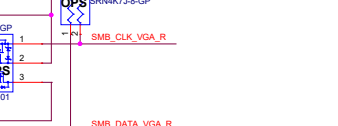
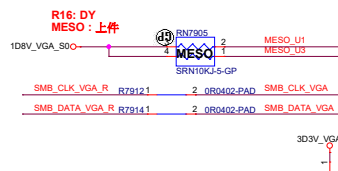
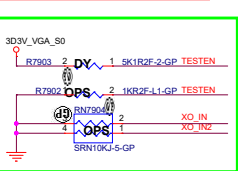


???
Difference with AMD



Debug only, for clock observation, if not needed, DNI

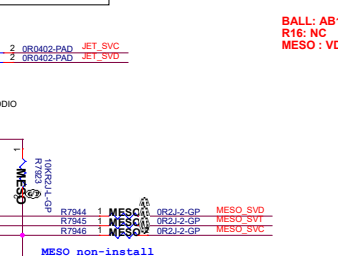




Pre-PWROK METAL VID CODES

	SVC	SVD	Output Voltage
	0	0	1.1
	0	1	1.0
a	1	0	0.9
	1	1	0.8

AMD suggestion	1	0	0.9
	1	1	0.8

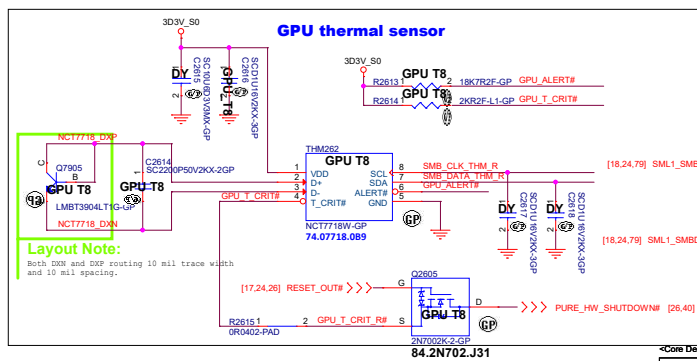
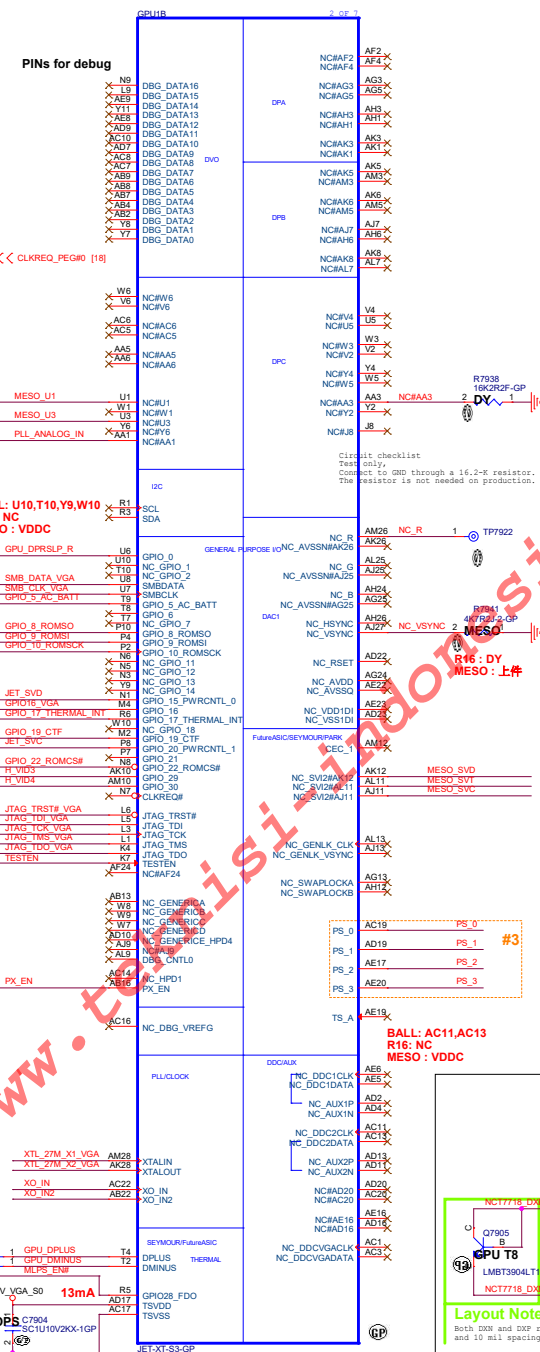


	SVID	PWR Sequencing
R16	R7919 R7920	PR8611 PC8607 / PR8612 PC8612

SVC	SVD	Voltage Selected (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

R _{pu} (Ω)	R _{pd} (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.



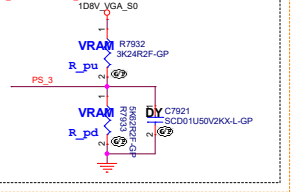
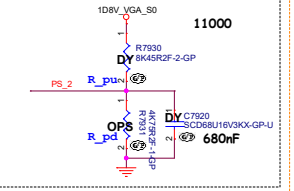
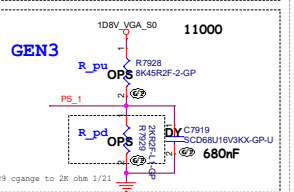
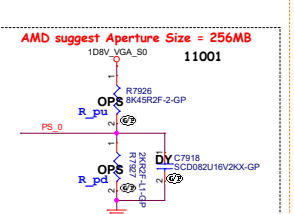
Value (nF)	Bits [5:4]
00	00
01	01
10	10
11	11

PS_O	R_pu	R_pd	Bits[3:1]	Size of the Prima
	NC	4750	000	128 MB
	8450	2000	001	256 MB
	4530	2000	010	64 MB
	6980	4990	011	Reserved
	4530	4990	100	N/A
	3240	5620	101	N/A
	3400	10000	110	N/A
	4750	NC	111	N/A

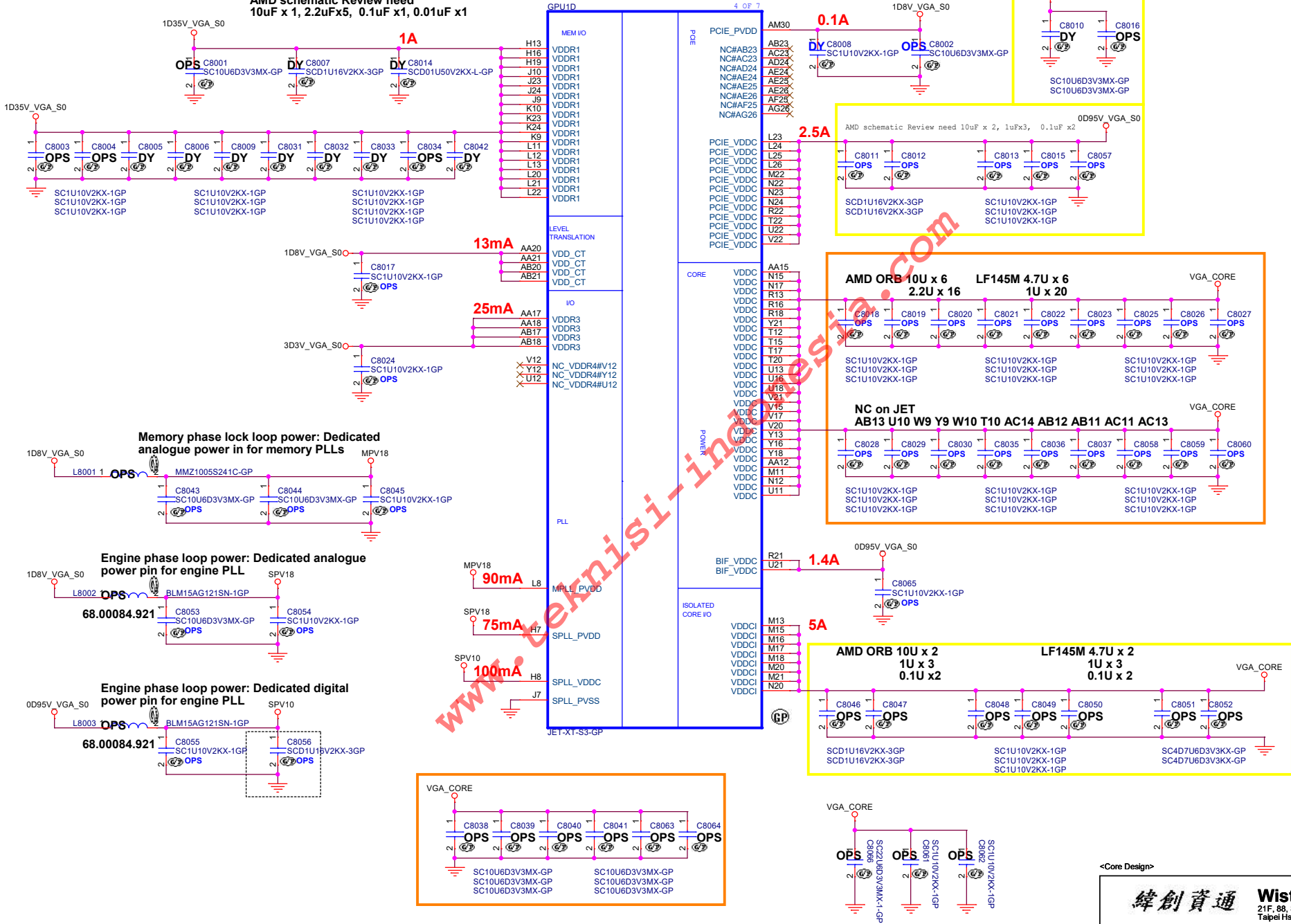
PS	R_pm	R_pd	Bits(3:1)	
NC	4750	000		RTC GEN1 is not supported - The CLUDGE05 power management capabilities is disabled
8450	2000	001		PC GEN1 is supported - The CLUDGE05 power management capabilities is disabled
8250	2000	100		PC GEN1 is not supported - The CLUDGE05 power management capabilities is disabled
6950	4990	011		PC GEN1 is supported - The CLUDGE05 power management capabilities is enabled
4550	4990	100		N/A
3040	5620	101		N/A
3400	10000	110		N/A
4750	NC	111		N/A

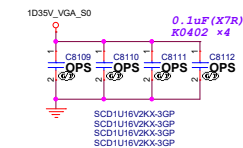
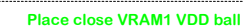
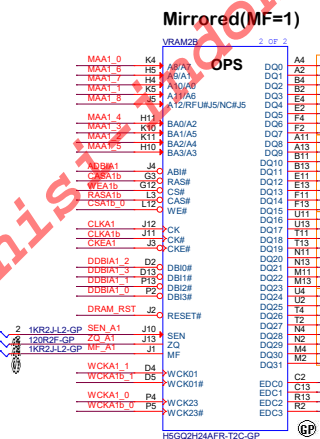
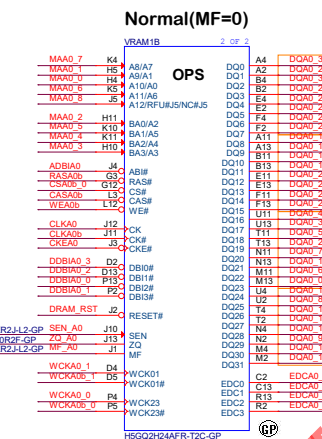
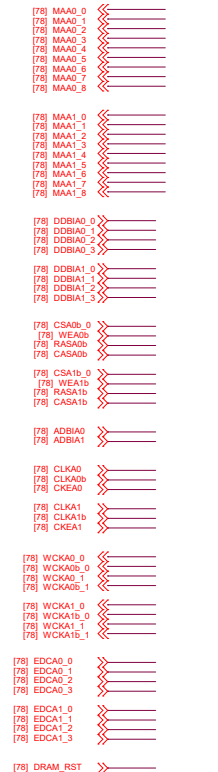
PS 2	R_in	R_pd	Bits[3:1]	
	NC	4750	000	Enable the external BIOS ROM device.
	8450	2000	001	N/A
	4530	2000	010	N/A
	6980	4990	011	N/A
	4530	4990	100	Enable the external BIOS ROM device.
	3240	5620	101	N/A
	3400	10000	110	N/A
	4750	NC	111	N/A

MLPS Memory ID setting:									
Board config[2:0]	Memory Type	Configuration	Row x Col x Bank bits	Channel Size	Vendor PN	Watson PN	SMT quantity	R_pu R7932	R_pd R7933
0	000	Samsung - GDDR5	256M x 32 bits	2GB	K4G80325FB-HC2B	N1M4MH		NC	4750
1	001	Micron - GDDR5	256M x 32 bits	2GB	MT51U256M32HF-70A	V15MH		8450	2000
2	010	SK Hynix - GDDR5	256M x 32 bits	2GB	H5G082H24M1R-R0C	029XX		4530	2000
3	011								
4	100								
5	101								
6	110								
7	111								



AMD schematic Review need
10uF x 1, 2.2uF x5, 0.1uF x1, 0.01uF x1





SSID = Vram (GDDR5)

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Title

GPU-VRAM3,4 (2/4)

Size
A4

Document Number

Turis/Vegas MLK AMD SR/ BR (FP4)

Rev
X00

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Title

GPU-VRAM5,6 (3/4)

Size
A4

Document Number

Vegas SKL/KBL-U

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A00

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Title

GPU-VRAM7,8 (4/4)

Size
A4

Document Number

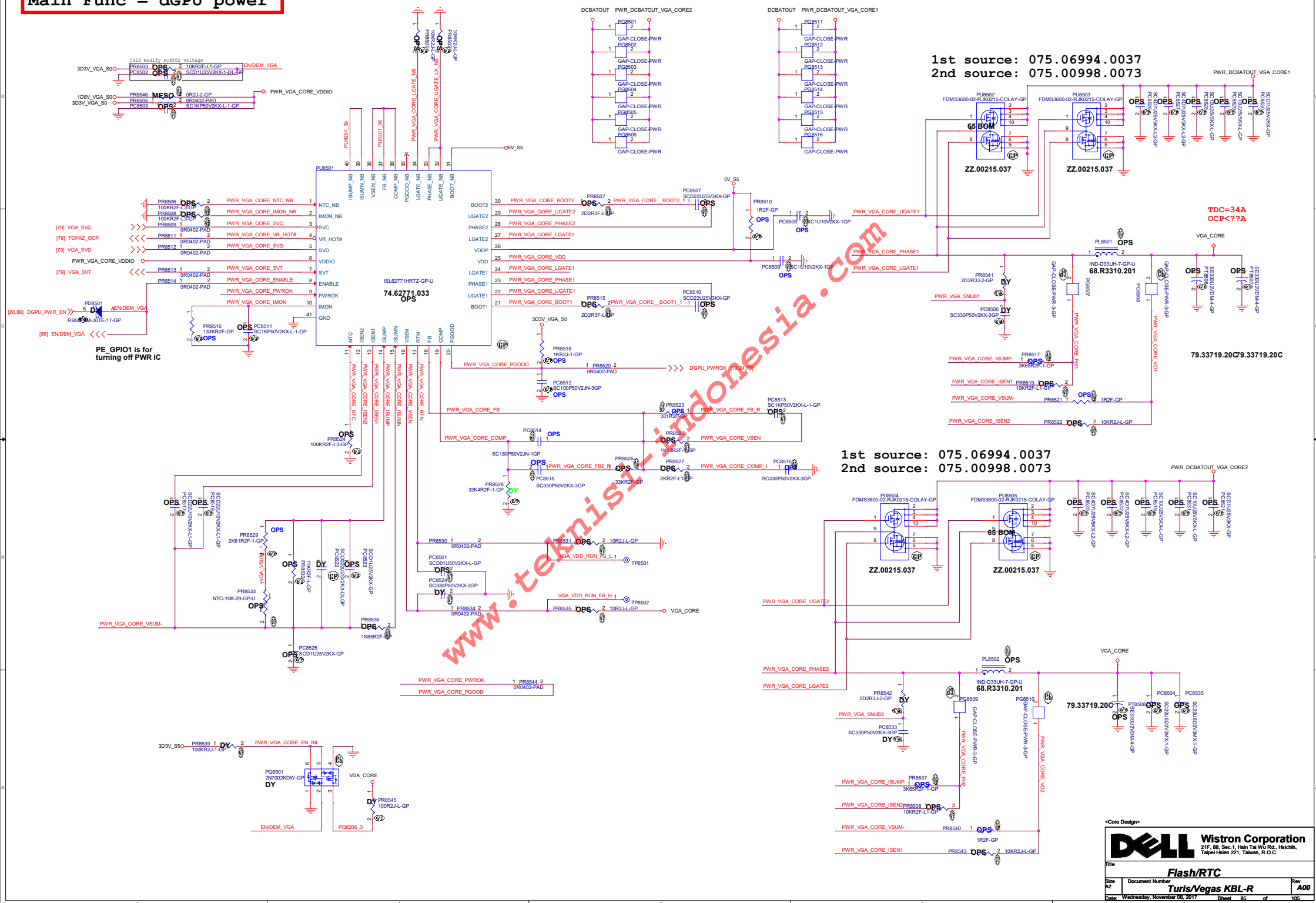
Vegas SKL/KBL-U

Rev
A00

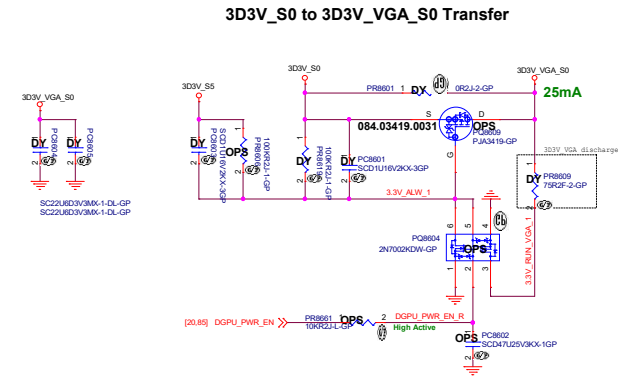
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Main Func = dGPU power



Main Func = dGPU



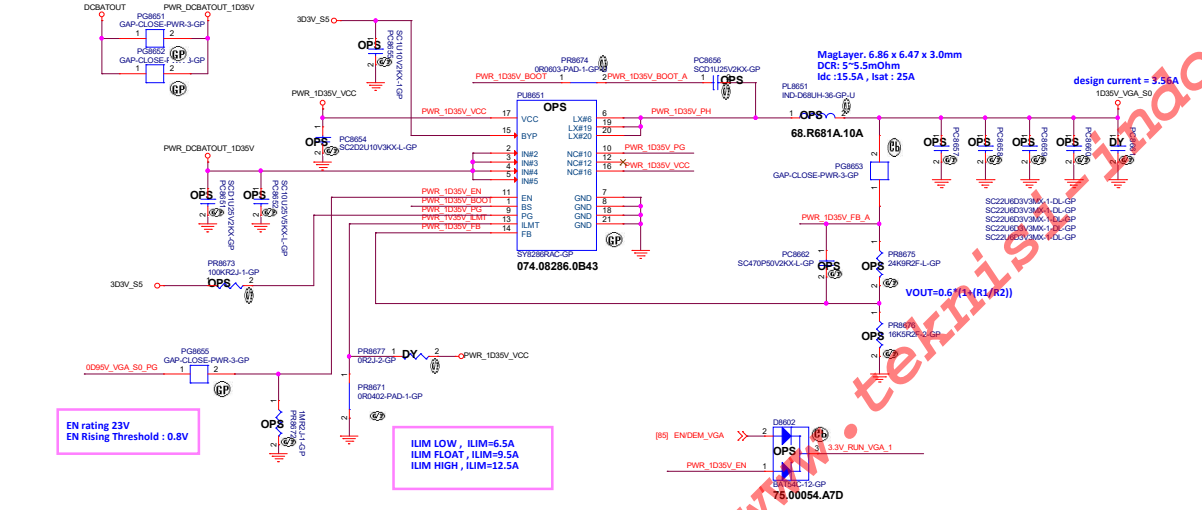
GPU PWR Sequencing

3D3V_VGAS0
=> 0D95V_VGA_S0/1D8V_VGA_S0
=> 1D5V_VGA_S0
=> VGA_CORE

All the ASIC supplies must reach their respective nominal voltages within 20ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50mV/us.

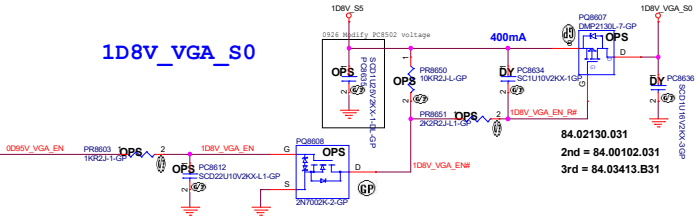
It is recommended that the 3.3V rail ramp up first.

It is recommended that the 0.95V rail reach at least 90% of its normal value no later than 2ms from the start of VDDC ramping up.



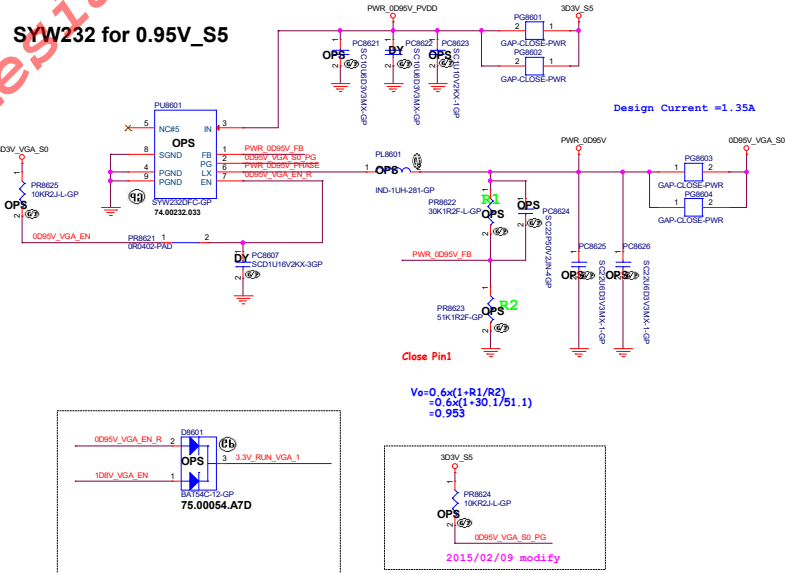
EN rating 23V
EN Rising Threshold : 0.8V

ILIM LOW , ILIM=6.5A
ILIM FLOAT , ILIM=9.5A
ILIM HIGH , ILIM=12.5A



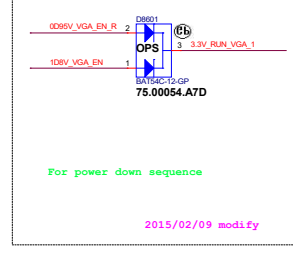
84.02130.031
2nd = 84.00102.031
3rd = 84.03413.B31

SYW232 for 0.95V_S5



Design Current = 1.35A

$V_o = 0.5 \times (1 + R1/R2)$
 $= 0.5 \times (1 + 30.1/51.1)$
 $= 0.953$



For power down sequence

2015/02/09 modify

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Reserved			
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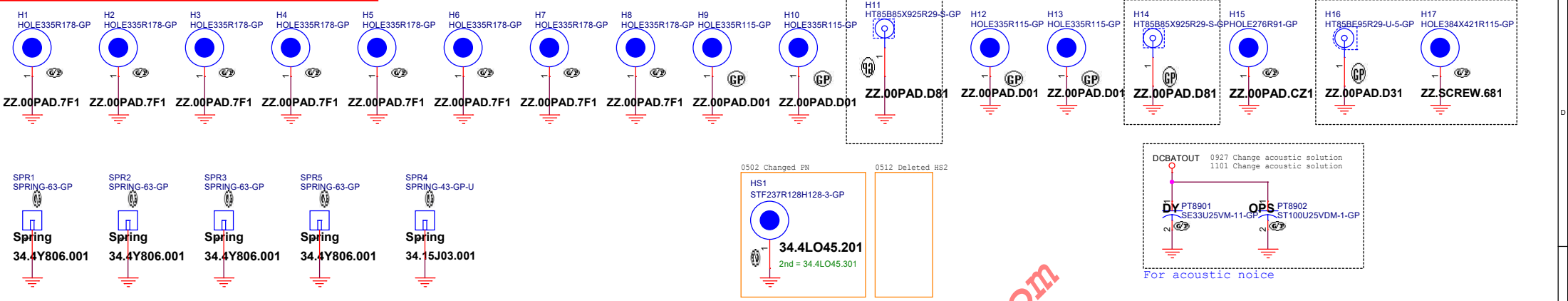
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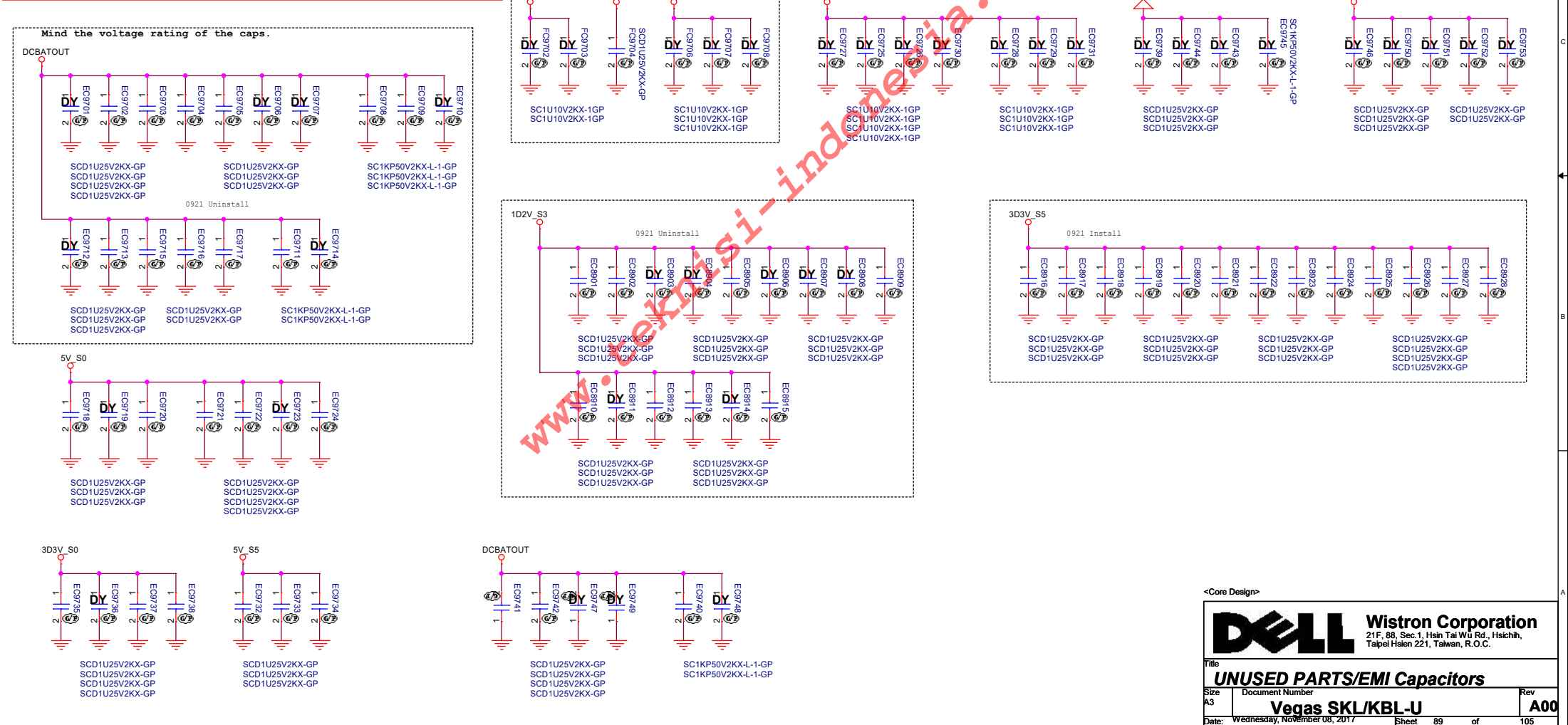
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Main Func = UnusedParts



Main Func = EMI & RF Capacitors



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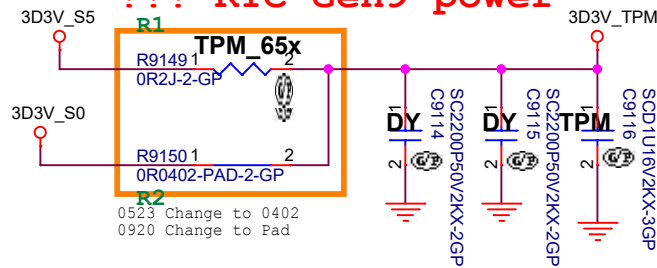
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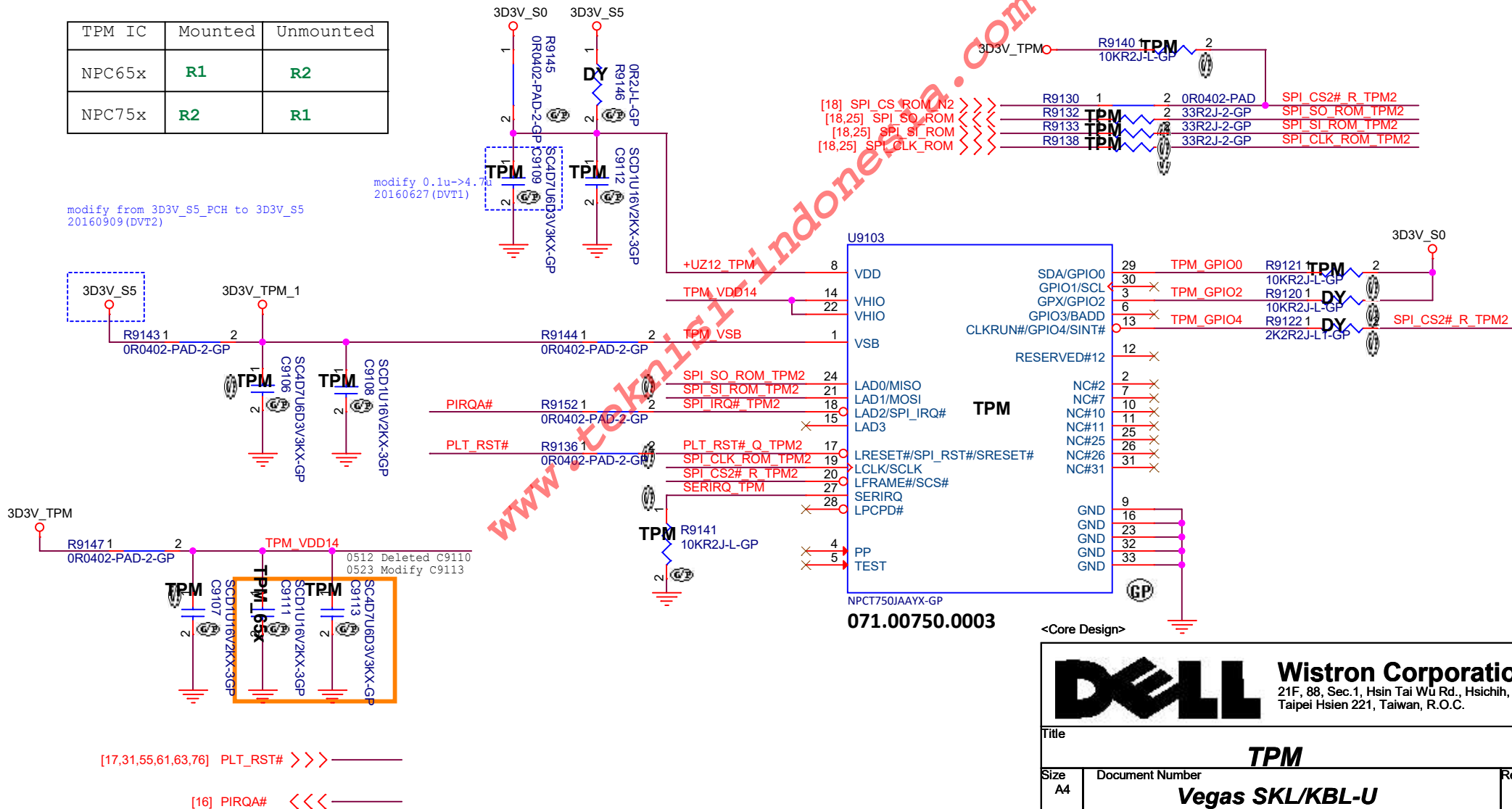
SSID = TPM

??? RTC Gen9 power



TPM IC	Mounted	Unmounted
NPC65x	R1	R2
NPC75x	R2	R1

modify from 3D3V_S5_PCH to 3D3V_S5
20160909 (DVT2)



	NPCT650		NPCT750	
Pin define	Power Name	Power status	Power Name	Power status
Pin1	VSB	VALW	VSB	VALW
Pin8	VDD	VRUN	VHIO	VRUN (S0)
Pin14	VHIO	VSPI	NC	nc
Pin22	VHIO	VSPI	VHIO	VRUN (S0)

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TPM

Size A4

Document Number

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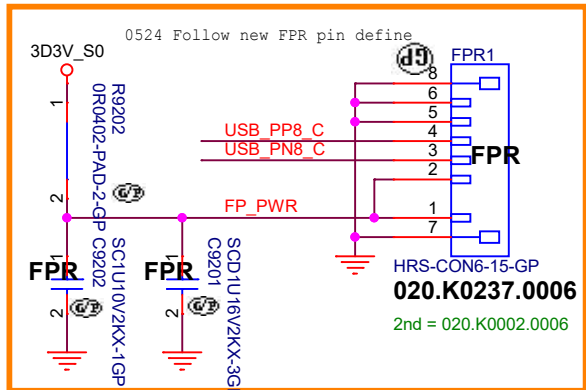
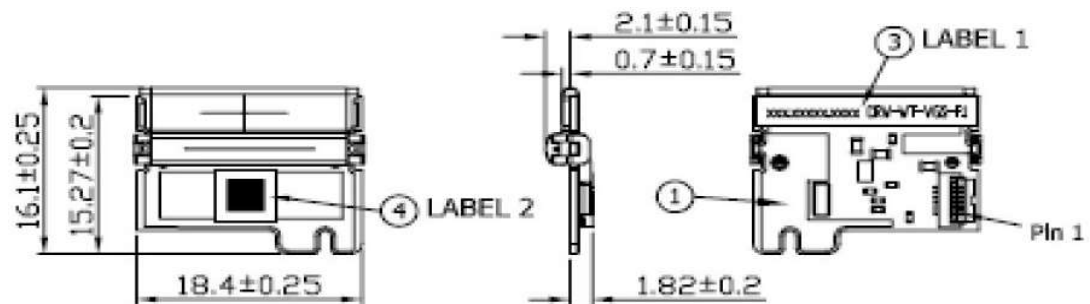
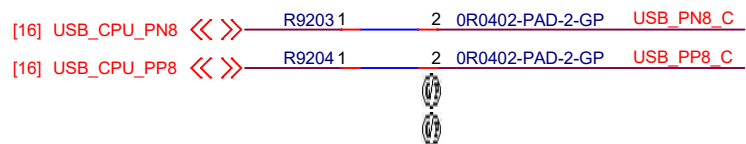
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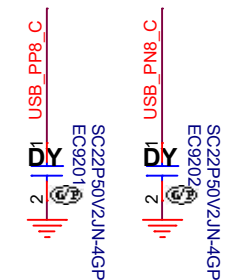
SSID = Finger Print



FingerPrint Pin Assignments.

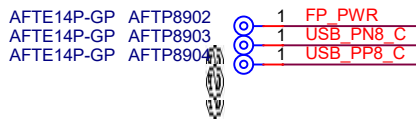
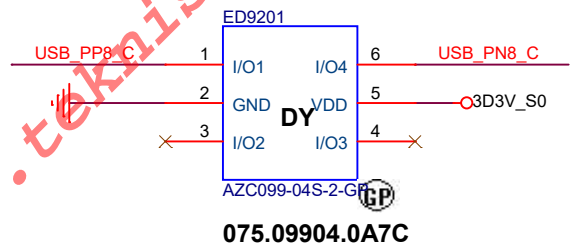
- Pin 1 = 3.3Vin
- Pin 2 = (ND)
- Pin 3 = D-
- Pin 4 = D+
- Pin 5 = Reset_N
- Pin 6 = GND

For EMI Reserved




Layout Note:

close to FPR1



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Title

LVDS_Switch

Size
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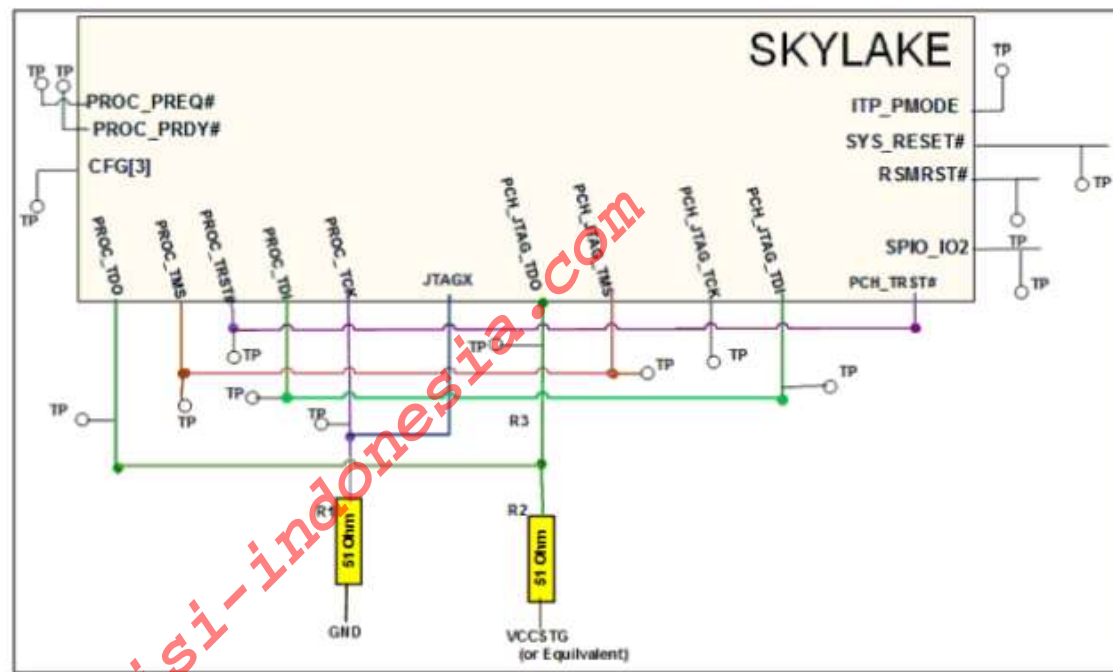
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Title CRT Switch			
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PCH_JTAG_TMS test point
XDP_TMS test point
PCH_JTAG_TDI test point
XDP_TDI test point
XDP_TCLK test point
XDP_TCK_JTAGX test point
XDP_TDO_CPU test point
PCH_JTAG_TDO test point



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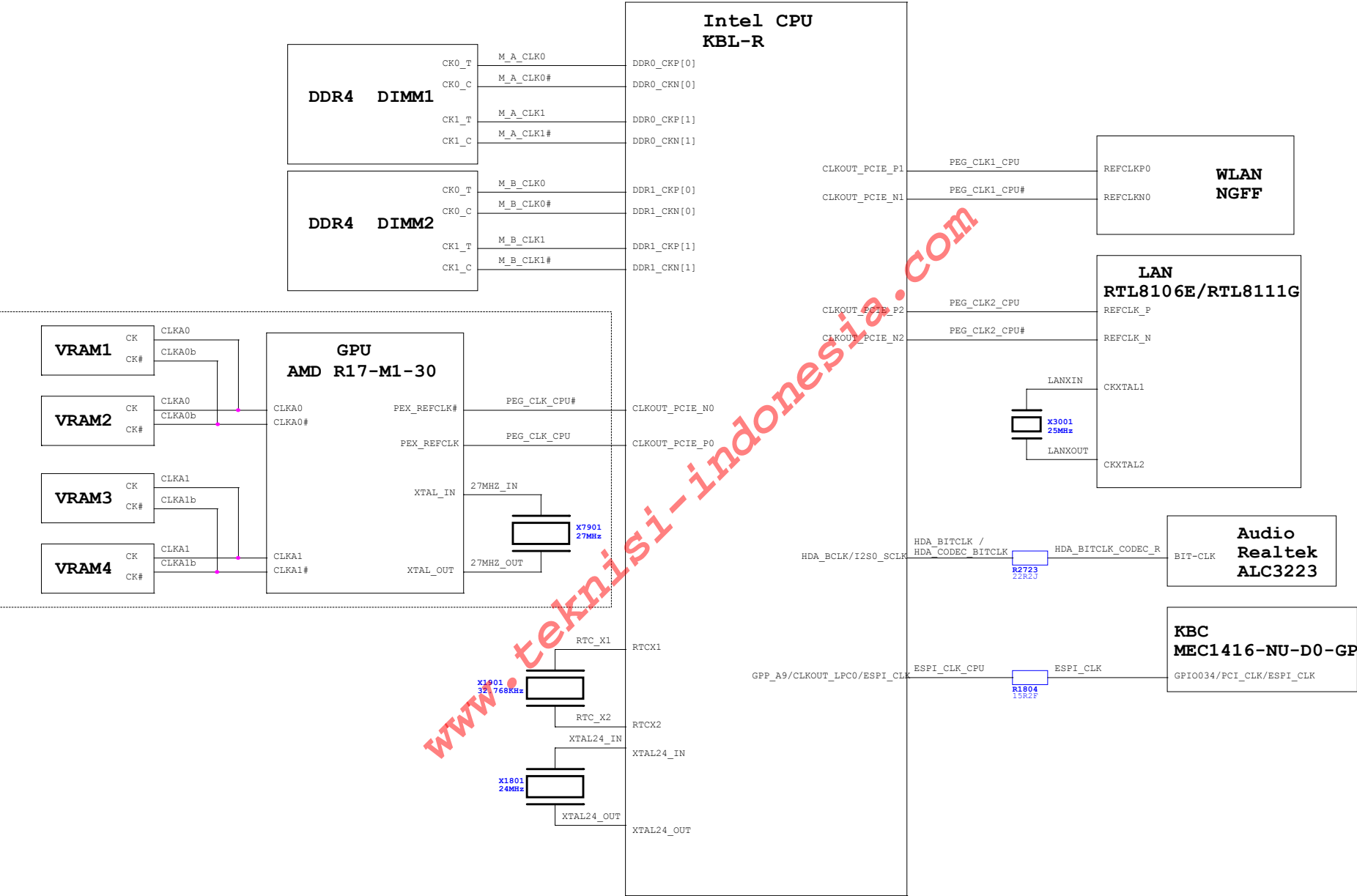
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Title
Debug (XDP debug)

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CLK Block Diagram



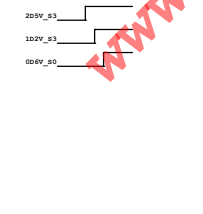
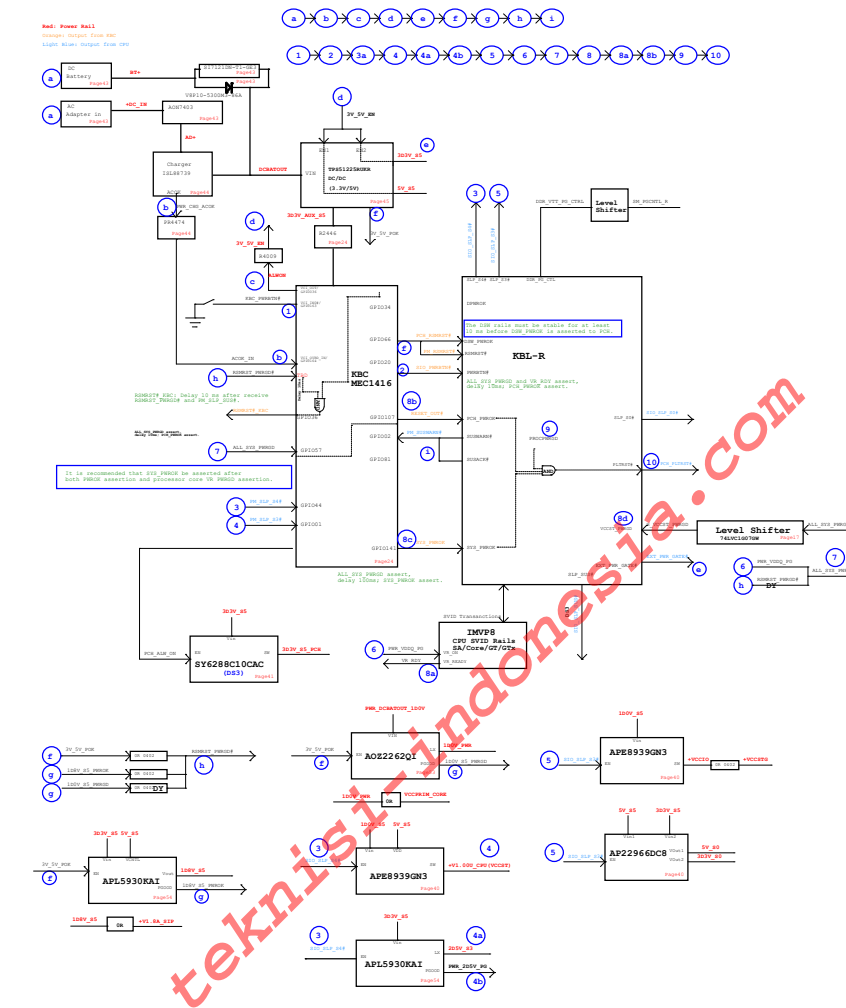
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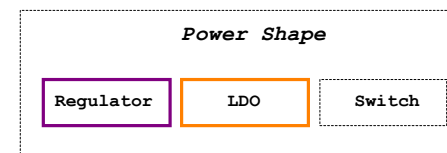
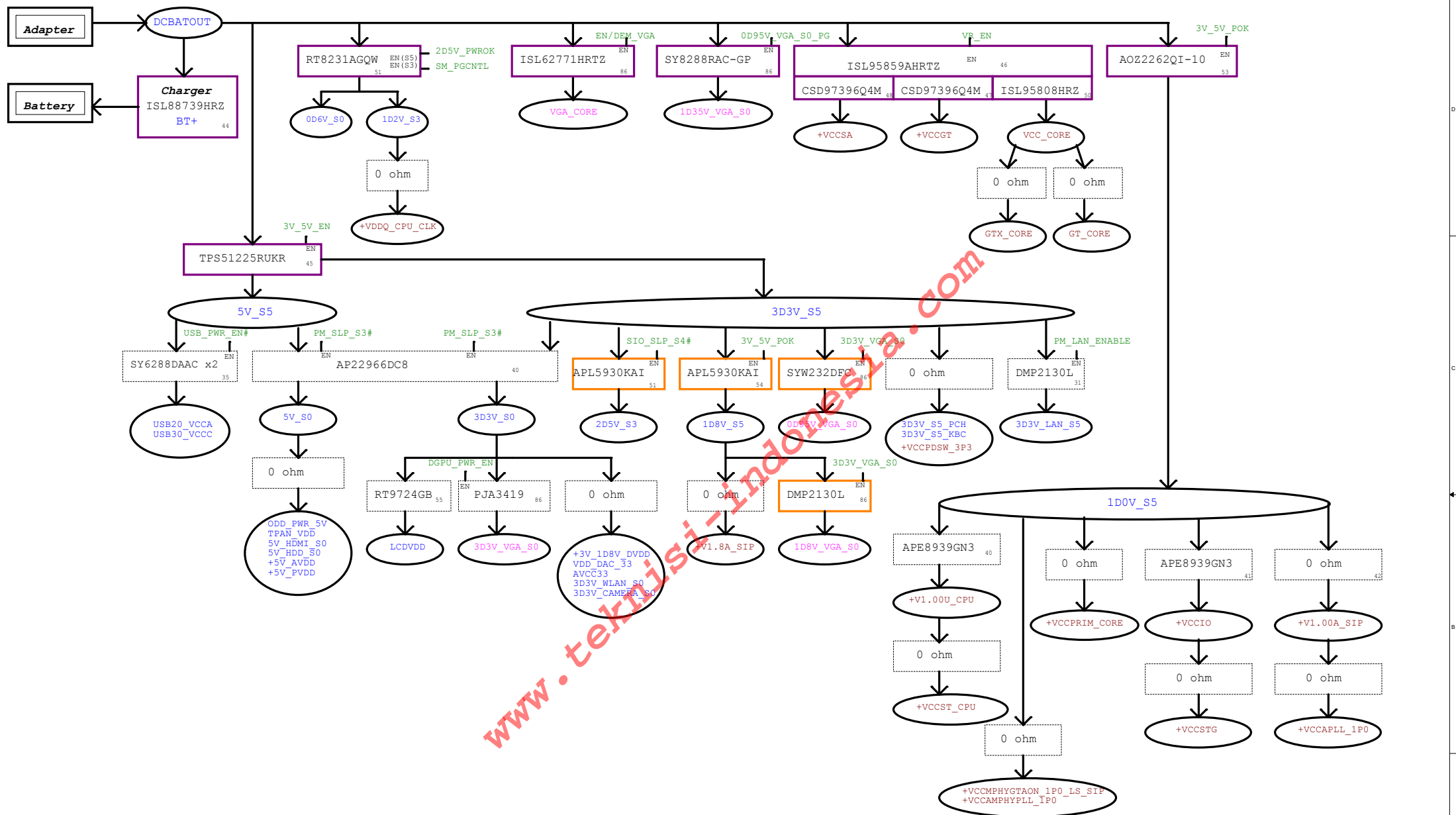
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Change History

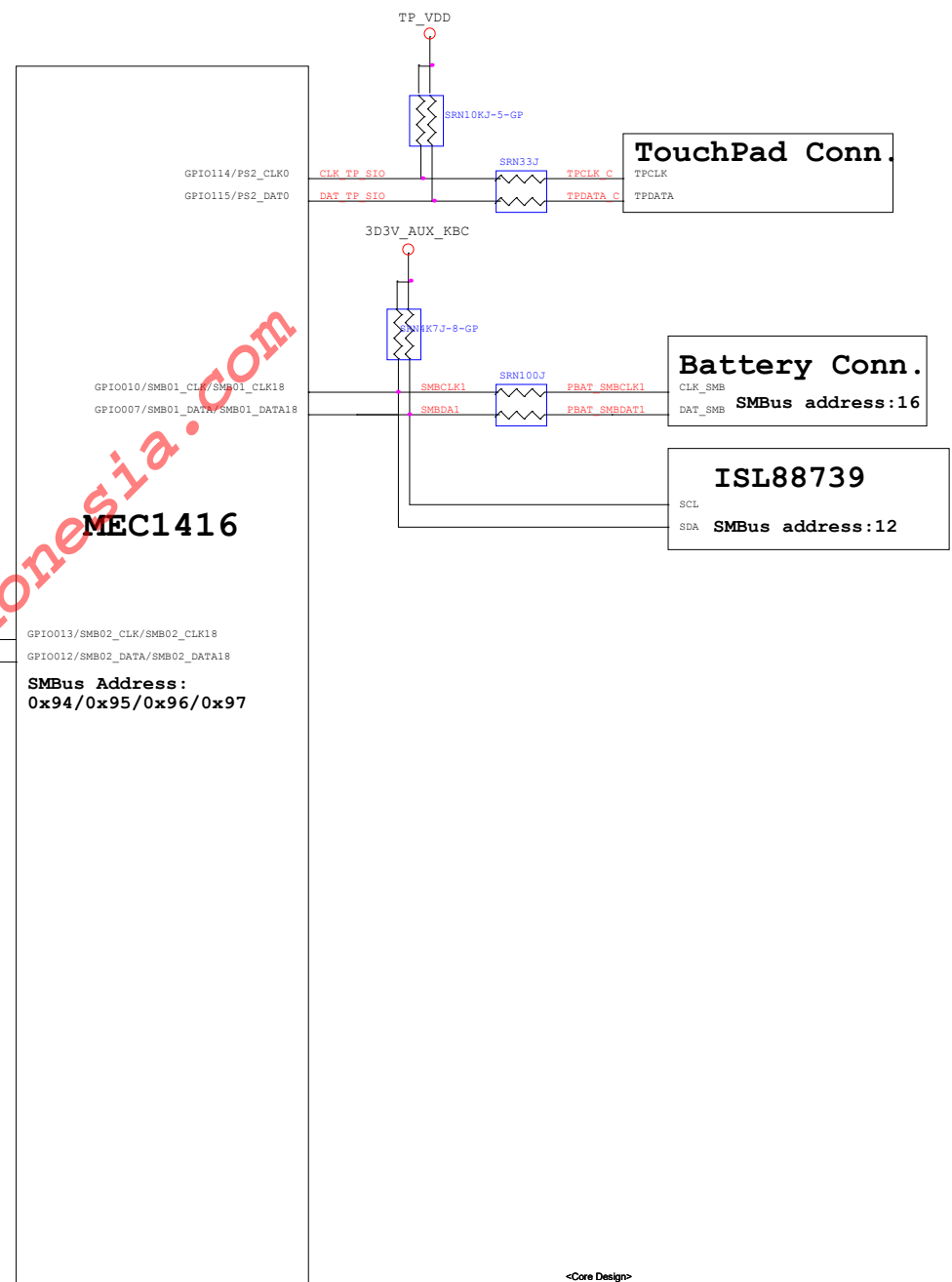
Vegas SKL/KBL-U

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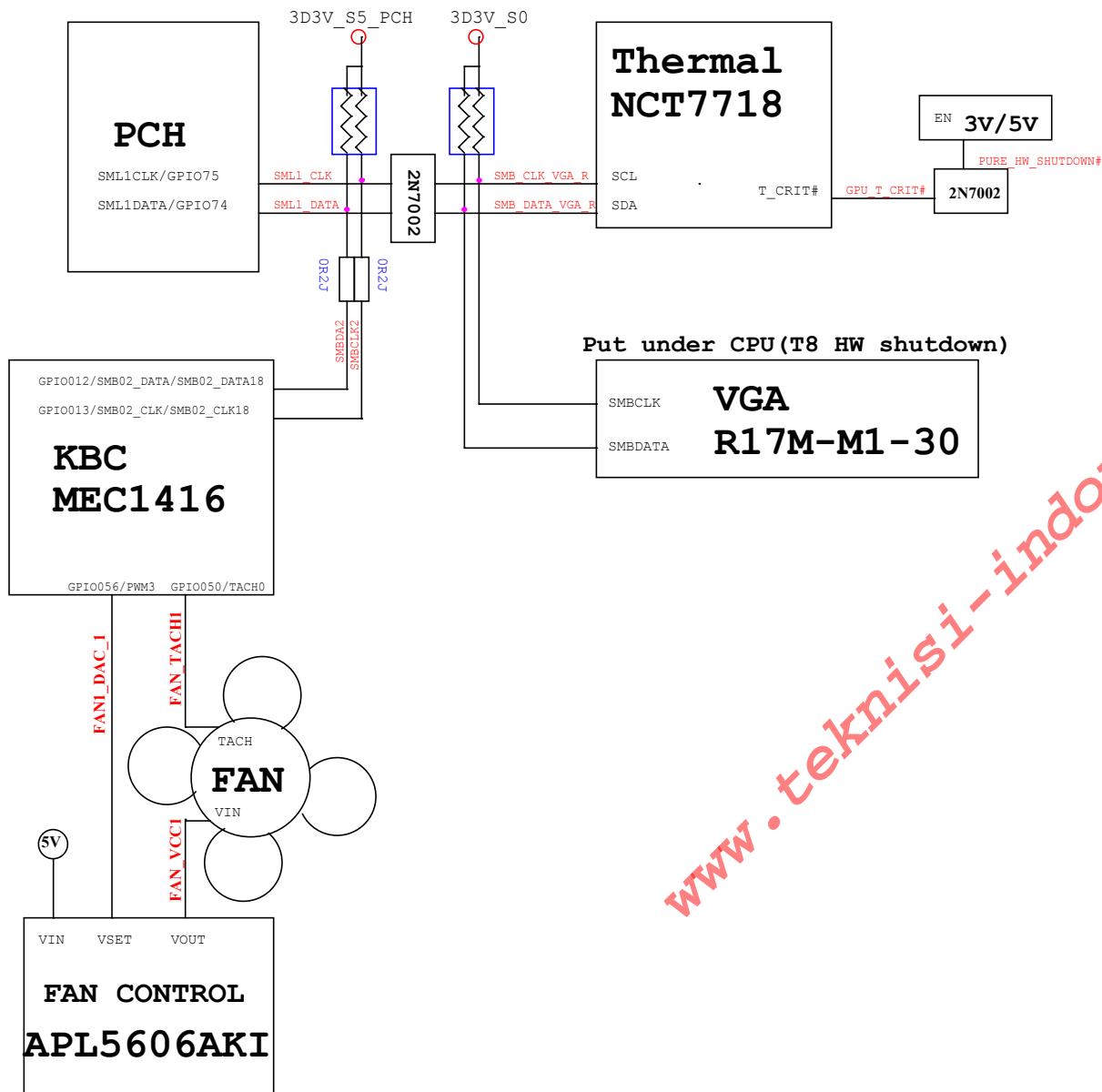




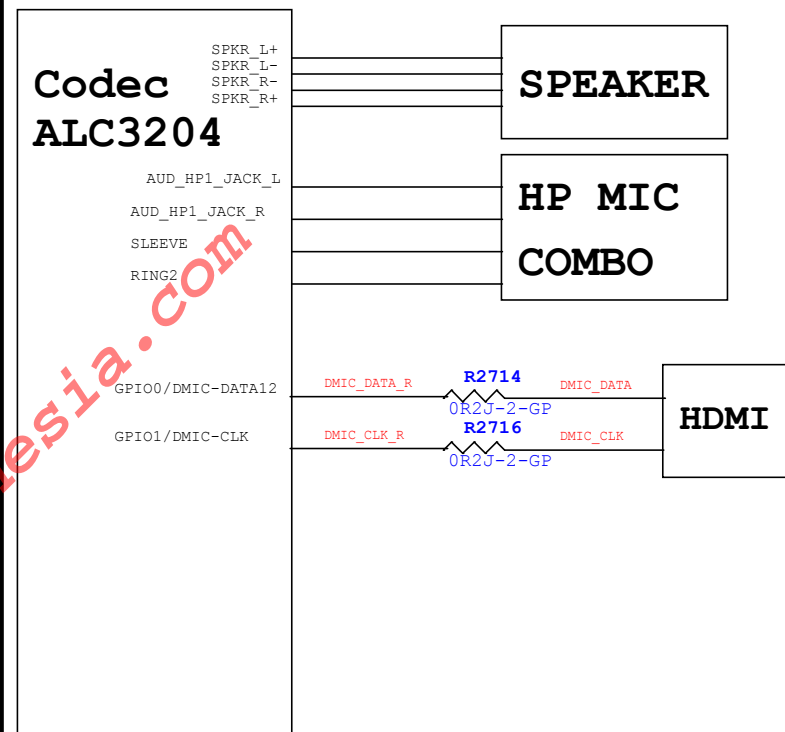
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



<Core Design>

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